Where is the Packaging Technology Drifting? : Speed/Flexibility

Choon Lee I COO and CTO

Agenda

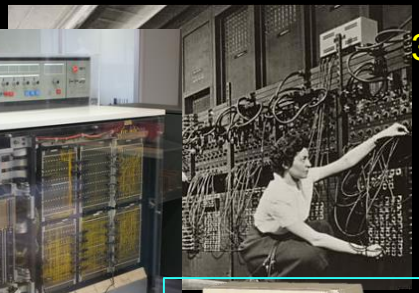
- Technology trend
- Amkor packaging solution
- New society proposal

Vacuum tube

ENIAC (Electronic Numerical Integrator And Computer) _ 1946

TRADIAC (TRAnsistor DIgital Computer) _ 1955

Transistor invention _ 1949 year



360 _ 1964

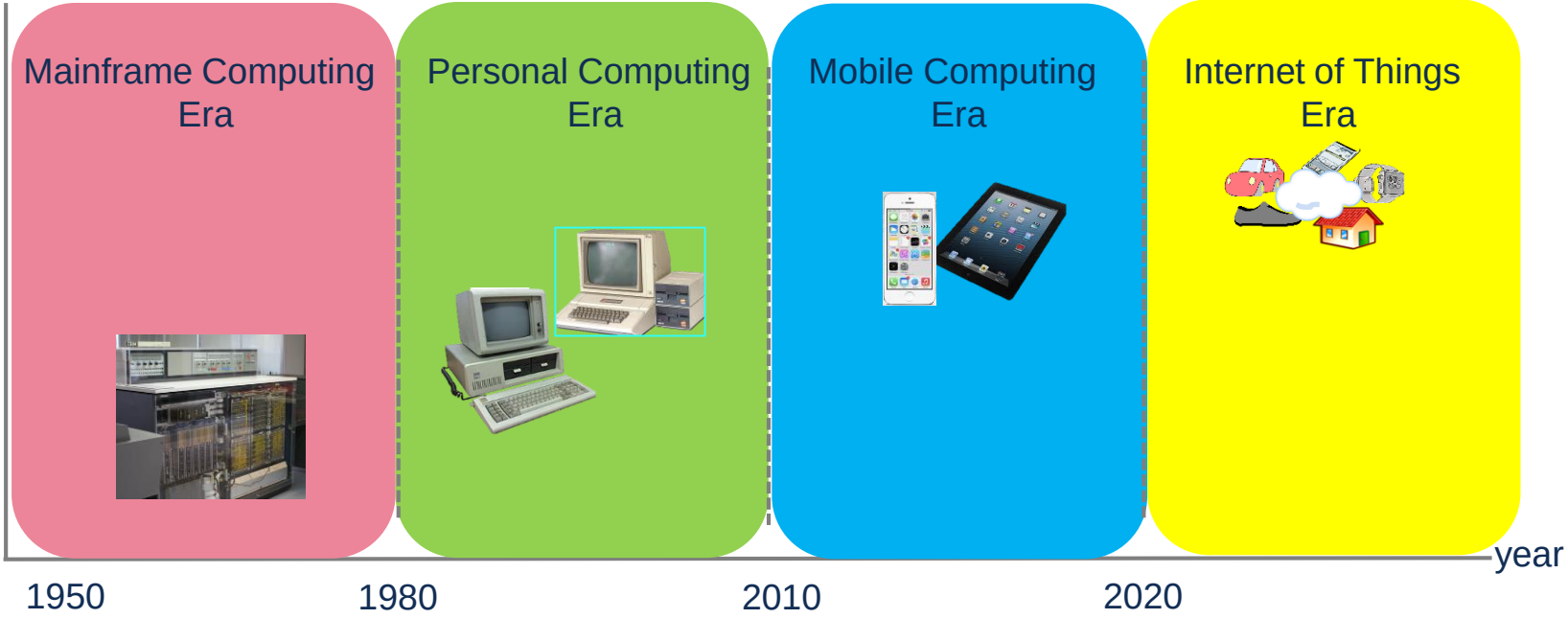
IC invention _ 1958 year

Apple II
_1977

VLSI introduction _ 1970s

Computing trend

market

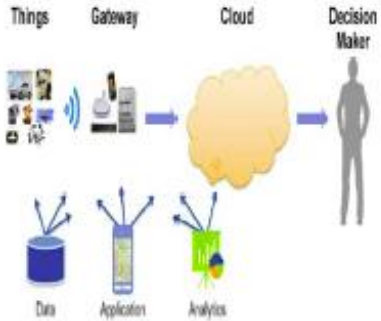


New growth driver

Price War

Competing hardware specs

With IoT

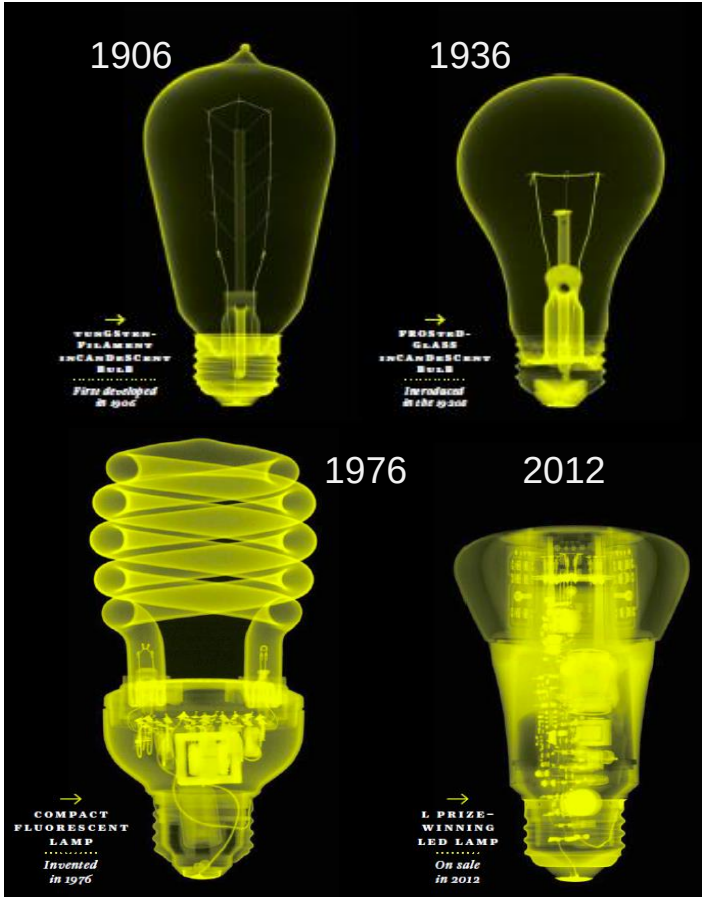


H/W innovation

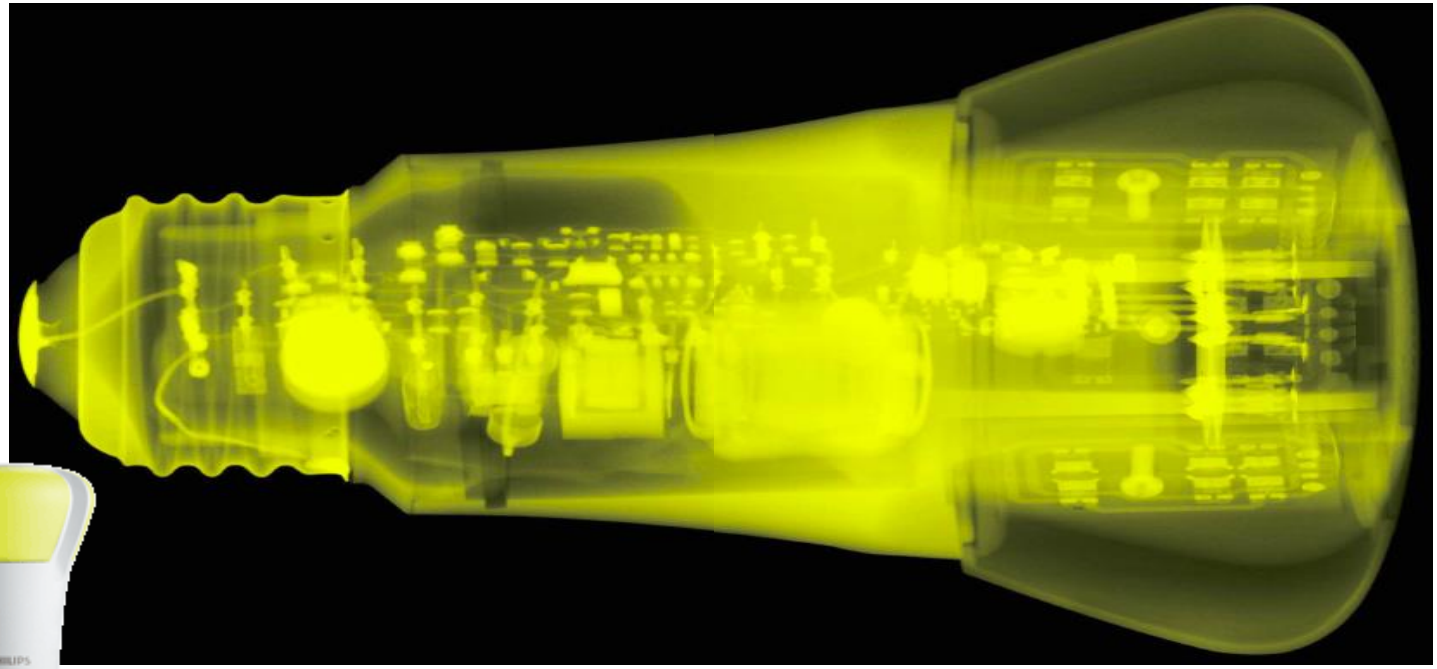
자료: HMC투자증권.

Electronics in Everything – The Light Bulb

- For 70+ years the common light bulb contained no electronics
- Then in the 1970's, CFL bulbs included a small power converter.
- Today the LED bulb contains a power supply, driver circuits, dimmers, etc.
- Soon bulbs will contain WiFi or Bluetooth radios and microcontrollers for remote operation.



X-ray Image of the L-Prize Winning LED Lamp



Glows white when illuminated

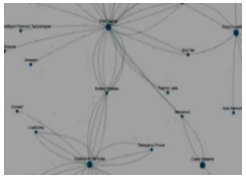
Philips Lighting

Q) What's the packaging solution for IoT era ?

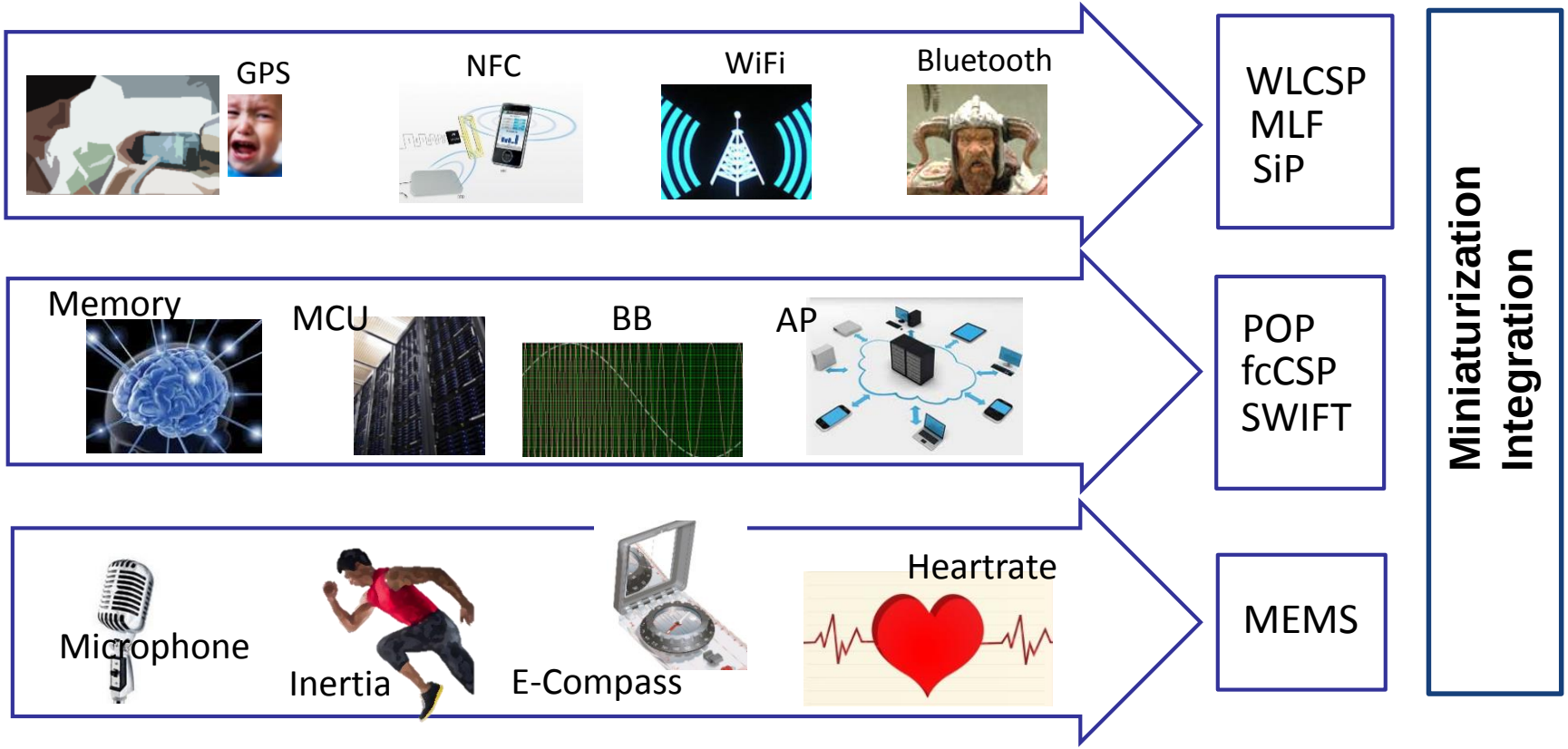
Electronics in Everything

+

IOT

Things	Transmission	Gateway	Big data	Decision
				

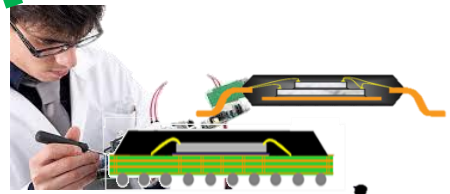
A) The answer is Miniaturization and Integration !



Q) What's the technology solution for new development paradigm?

Customer

Development



material

Equipment

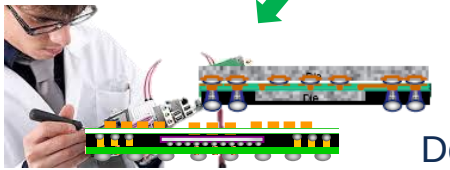
Yesterday

Time Interval
Debugging Time
Formalized

Today

No Time Interval
No Debugging Time
Flexible

Customer



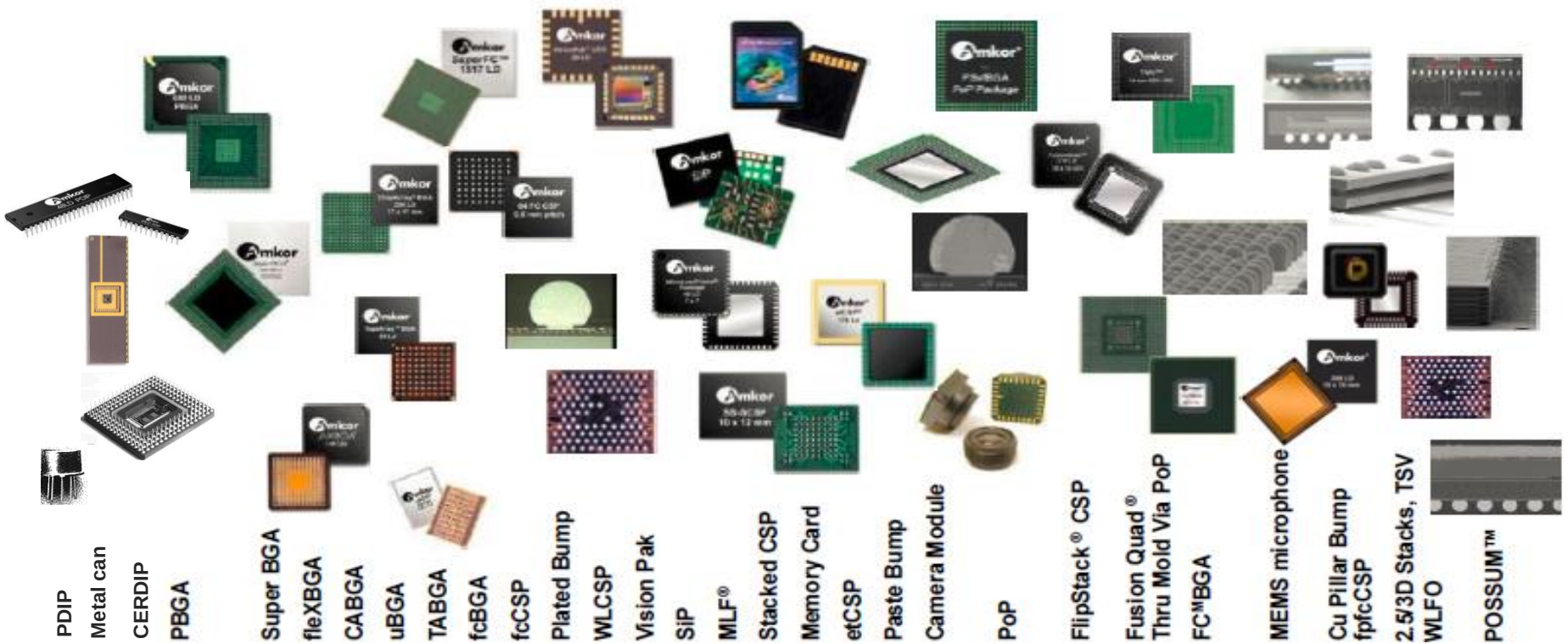
Development

material

Equipment

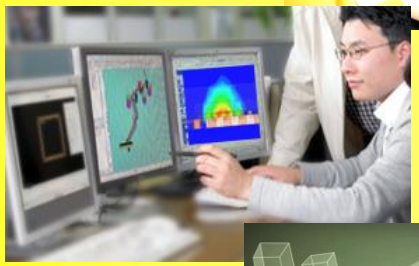
A) The answer is wide packaging experience and process readiness !

Amkor Packaging Experience



Amkor One-stop and Total Solution

Design

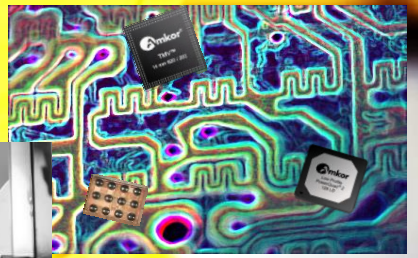


Simulation

Development

Production

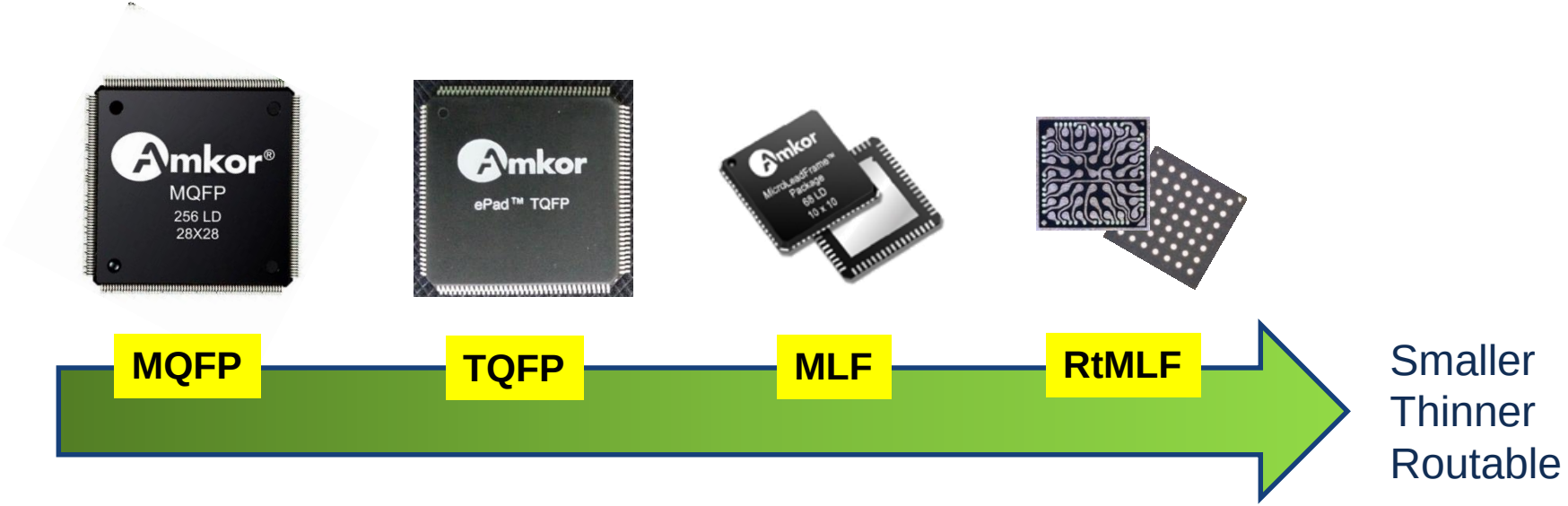
Analysis



Testing

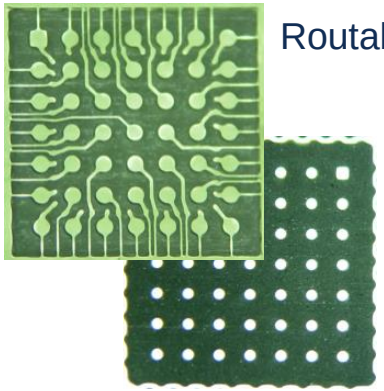
Leadframe Package Innovation

- Even matured leadframe package, the innovation named routable is achieved



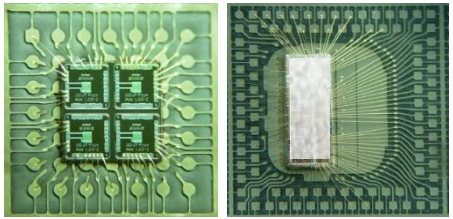
RtMLF (Routable MLF)

- **What is RtMLF?**
  - Resin filled trace available 1L substrate(MLF)
  - Low cost and small form factor driven structure
  - For server, PC, game console as well as mobile peripheral
- **Interconnection method**
  - Wire Bonding, Flip Chip
- **Development status**
  - Body size : ~10x10mm
  - I/O count : ~176

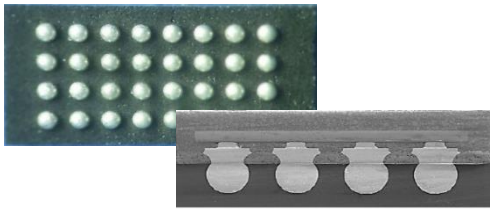


Routable

Out pad



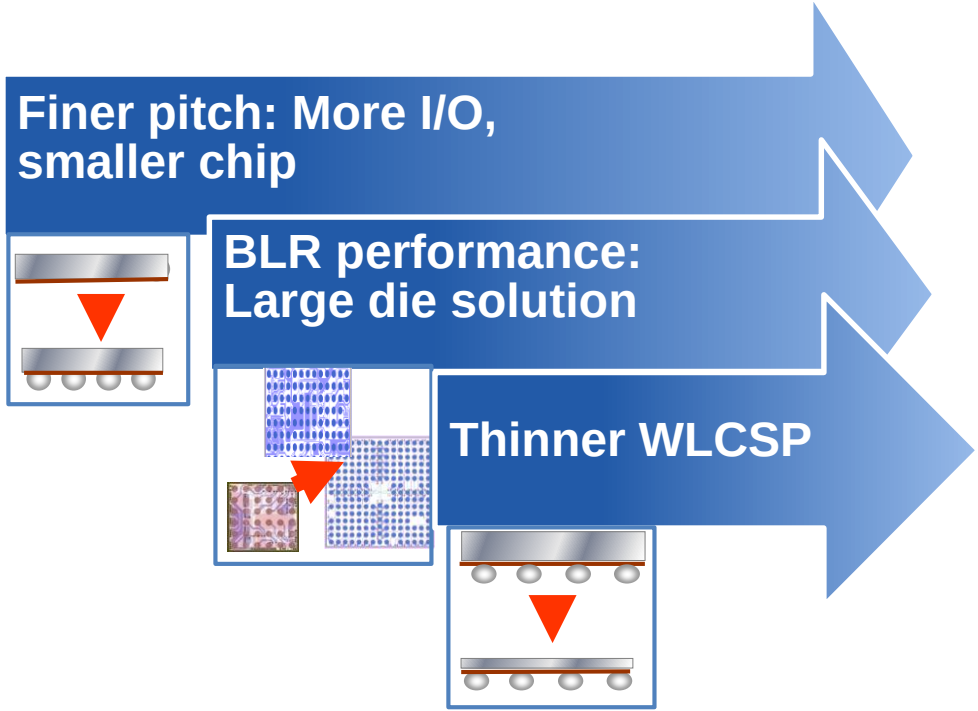
Wire Bonding

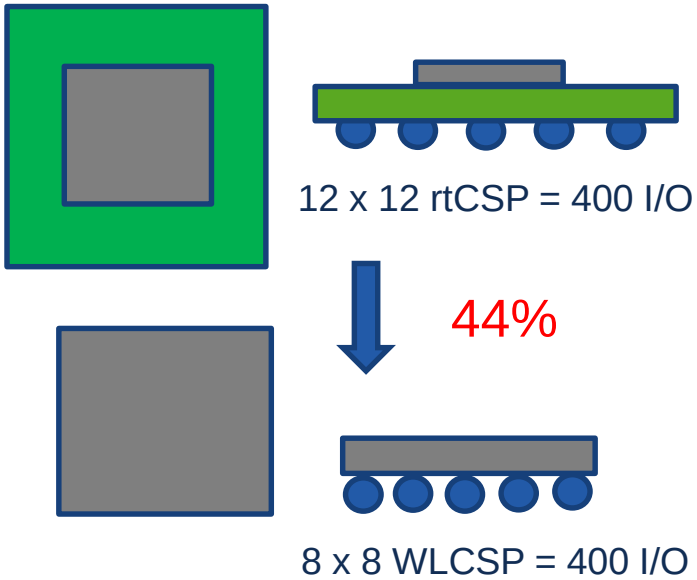


Flip Chip

WLCSP is moving

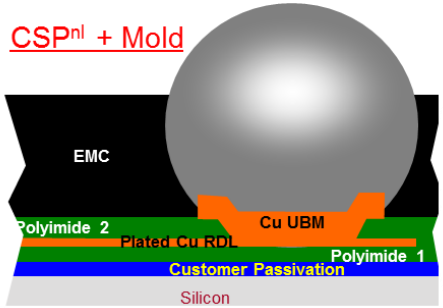
- Mid I/O packages are converted to WLCSP due to form factor/cost





WLCSP Large Die Solution

- **WLCSP with mold structure is to improve solder joint performance**



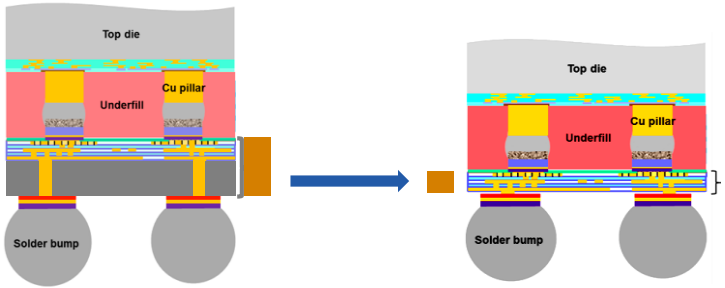
BLR performance Driven

BD size. (mm)	Die thick (um)	Ball size (um)	Ball Alloy	TC		Drop	
				1st fail	Mean life	1st fail	Mean life
10x10	350	250	SACQ	1225	2849	179	1228*
			SB05	836	1944	251	1442*

* **Mean life is extrapolated because failure ratio is less than 50%**

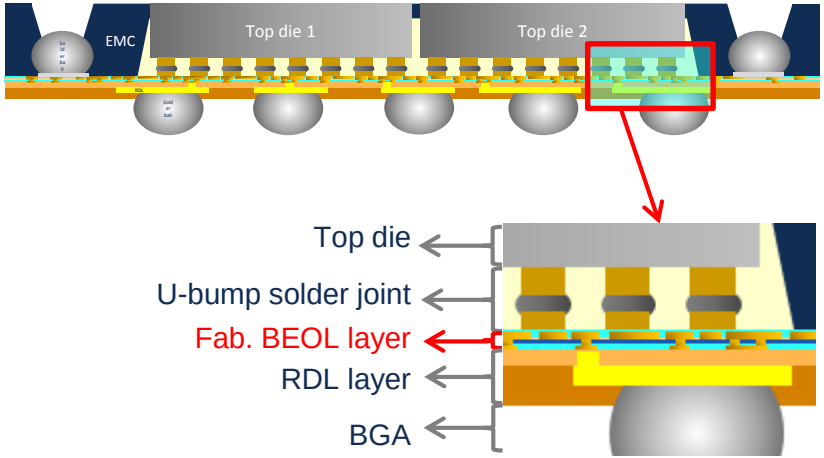
New Concept Technology without TSV

- Higher Performance
- Integration
- Cost benefit



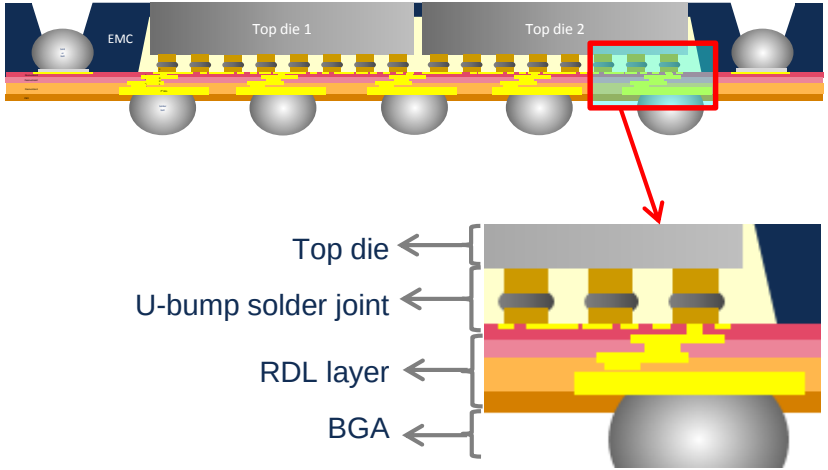
SLIM™

Silicon-Less Integrated Module



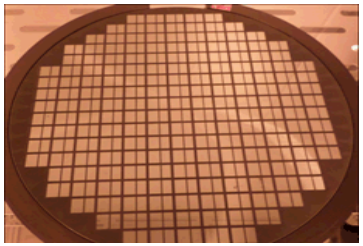
SWIFT™

Silicon Wafer Integrated Fan-out Technology

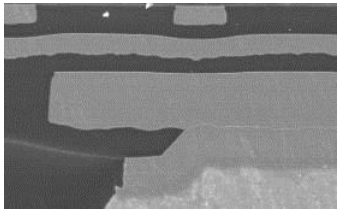


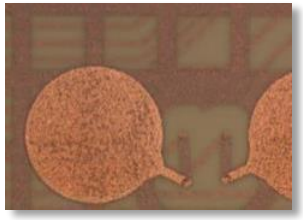
SWIFT covers Flip Chip CSP and SiP application

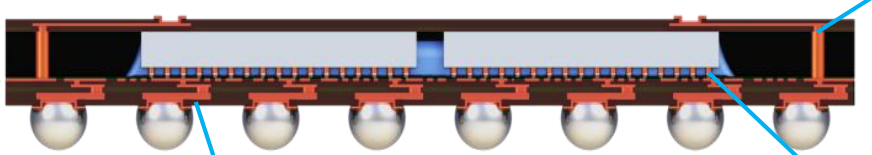
Molded 12inch CoW wafer processing
- Available



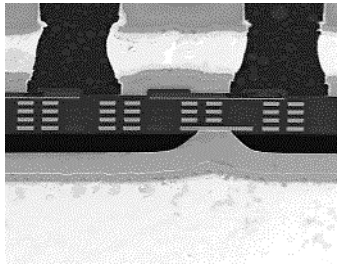
Fine L/S multi RDL
- 5/5um available
- 3L RDL demonstrated



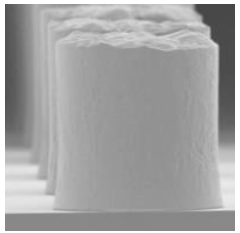




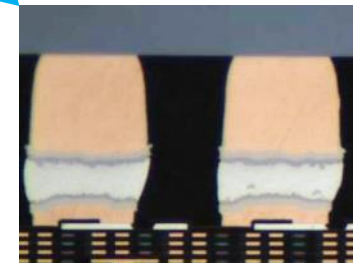
Backside pattern reveal and carrier attach
- Available



Tall Cu pillar for memory interface
- 180um tall Cu demonstrated



Fine pitch u-bump interconnection
- CoW chip attach with mass reflow
- 40/45um available
- 30um demonstrated

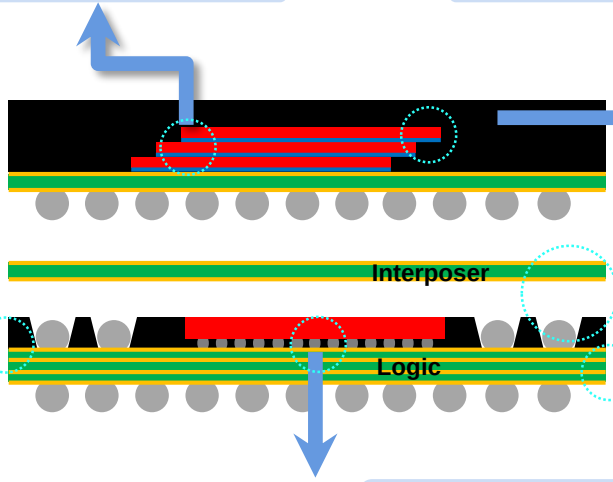


Logic and Memory package stack

Body size
- 8~17mm

DAF
- 5um thick

Thin die
- 20um thick



Mold
- MUF
- Exposed die
- Bare die
- Strip grinding

High memory I/O
- Fan-in PoP
- Fine pitch TMV (~0.2mm)

BGA ball pitch
- 0.35mm/0.30mm

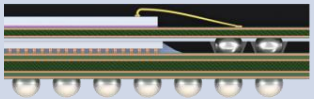
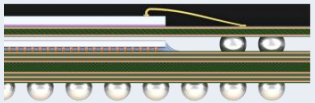
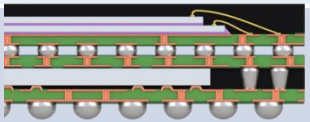
Interconnection
- Solder bump
- Cu pillar

Chip attach
- LAB
- TCNCP
- MR

Substrate
- ETS
- Coreless

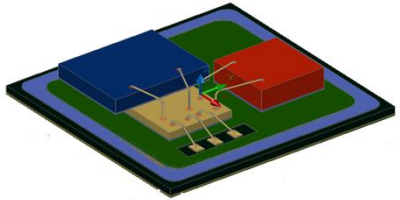
Thin PoP Roadmap

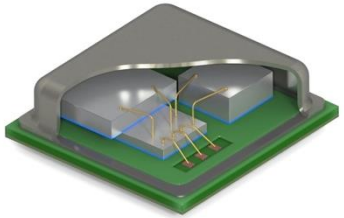
(max thickness)

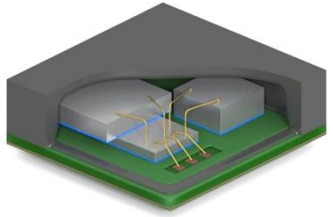
	Available	2015	2016	2017
Memory thickness (assumption)	0.43	0.39	0.36	0.35
Exposed die TMV 				
• Bottom PKG thickness	0.69	0.60	0.51	0.48
• Total stack-up thickness	1.12	0.99	0.87	0.83
Bare die TMV 				
• Bottom PKG thickness	0.69	0.65	0.63	0.62
• Total stack-up thickness	1.12	1.04	0.99	0.97
Interposer TMV 				
• Bottom PKG thickness	0.71	0.65	0.61	0.59
• Total stack-up thickness	1.20	1.10	1.04	1.00

Packaging Trend in Sensors is Going to Fusion!

Sensor	Trim Algorithm	Package	Package Attributes
3-Axis Magnetometer	Data Processing	Non-Ferromagnetic Package	Discrete Sensor Packages
3-Axis Accelerometer	Data Processing	Package	
3-Axis Gyro	Data Processing	Package	
Pressure Sensor	Data Processing	Cavity Package	
Misc: IR, Humidity Optical, Microphone	Sensor Fusion	Cavity Package	
Mag + Accel 6DOF eCompass Sensor	Sensor Fusion Reference Mapping & Trim Kalman Filter (or similar) Data Processing	Combo Sensor Package	**Fusion Packaging** • Multi-Die w/Interconnect • Low Stress
Accel + Gyro 6DOF Sensor			
Mag + Accel + Gyro 9DOF Sensor			
Mag + Accel + Gyro + Pressure 10DOF Sensor		Cavity Combo Package or Partial Cavity Package	• Cavity or Partial Cavity • Multi-Die w/Interconnect • Very Low Stress • Solid, Optical or Ported Lid
Misc: IR, Humidity Optical, Microphone			



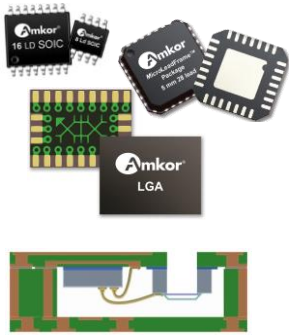




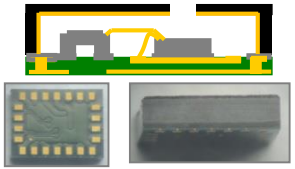
MEMS / Sensor Products

Available	2015	2016	2017

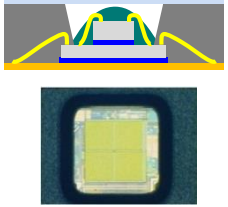
Overmold Laminate cavity



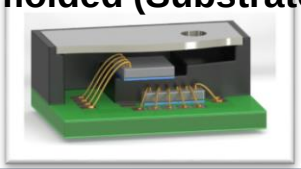
Polymer lid cavity



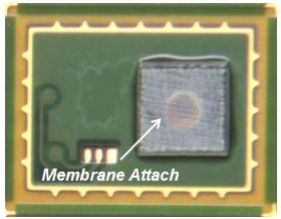
Exposed sensor



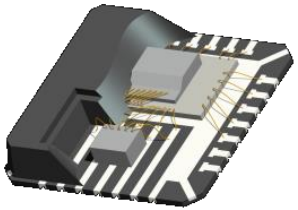
Pre-molded (Substrate)



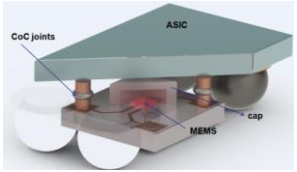
Membrane U-phone

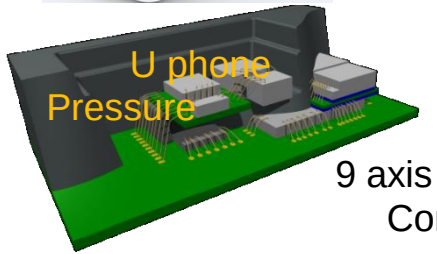


Pre-molded (Leadframe)



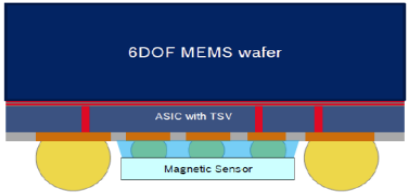
WLCSP MEMS





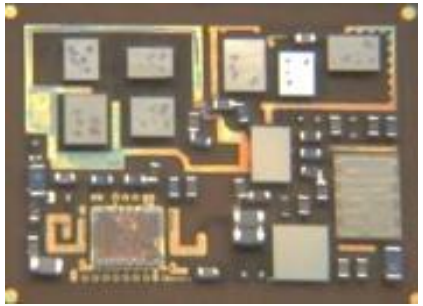
9 axis Inertial Combo

TSV possum sensor



SiP Requirement

Small form factor
- Low profile component (01005/008004)
- 150um Cu pillar



Conformal shield
- Sputtering

Package size
- 2.0x2.5~25x30 mm

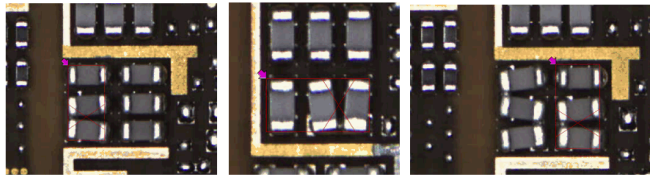
Interconnection
- Flipchip and Wirebond

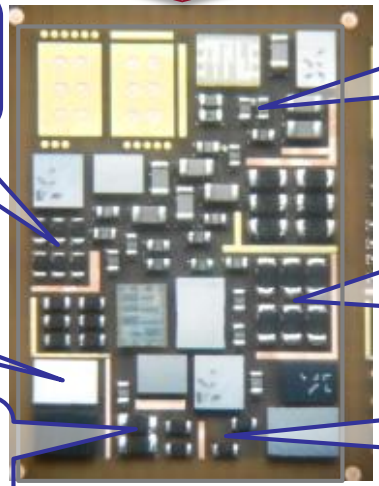
- **Possum**
- **Two side assembly**

Embedded passive

Advanced SiP Design Guideline

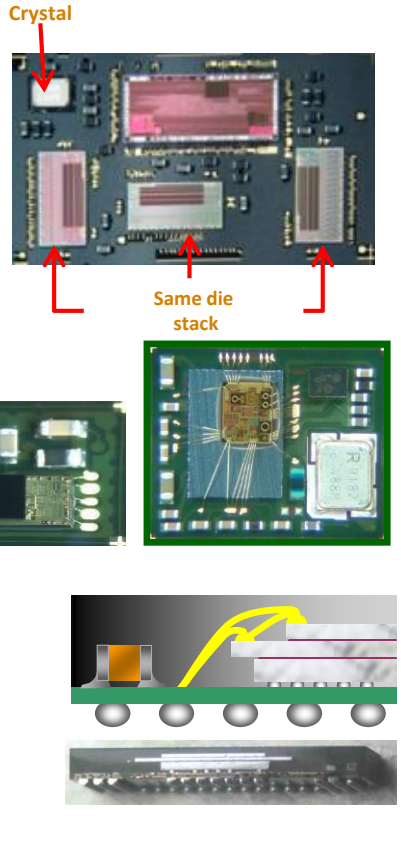
Item	Production	Development
Die to PKG Edge	85	75
Comp. pad to PKG edge	85	75
Die to Die	75	65
Non common net Comp. pad	85	75
Common net Comp.	60	50
Metal trace to Comp.	80	70





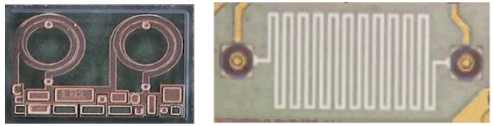
Amkor's Experience with Varying End Applications

- **Memory**
  - Same die stack, Pyramid stack, side by side MCM
  - DAF, FOW, Wire Bonding Interconnection
- **Connectivity, Digital, Consumer**
  - WLCSP (FC die) and Wire Bond Stack, Crystal
  - FC+ 2 die stack, die to die bonding, die to PCB bonding
  - MUF (Mold Under Filling)
- **Automotive, Sensor**
  - Sensor Die expose –Film assist molding
  - Double side assembly, Possum FC die
  - TSV, CoC stack

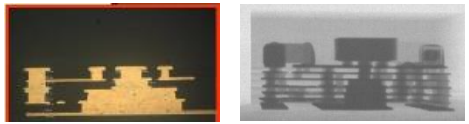


SiP Technology

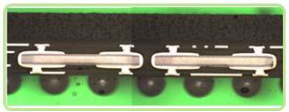
Available	2015	2016



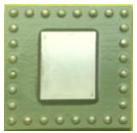
IPD (Customer consigned)



Core-Less Substrate Pkg



Embedded Passive / Die

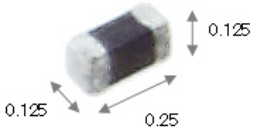


Possum FC

Two Side assy

Conformal Shield

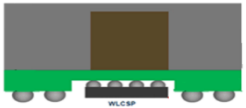
Compartment Shield



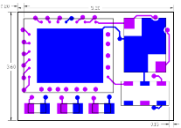
008004 Passive

Double side molding

Recessed Substrate

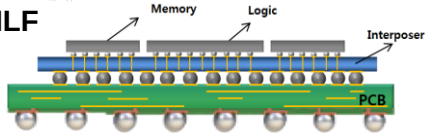


Cavity Substrate

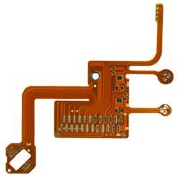


RtMLF

SLIM/SWIFT



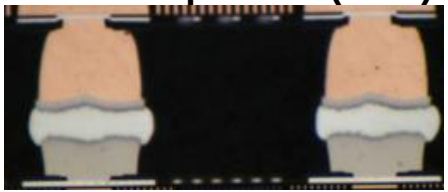
TSV



Flex Substrate

Si Photonics

- 20um diameter / 40um pitch
- 2~5K bump count (nom)



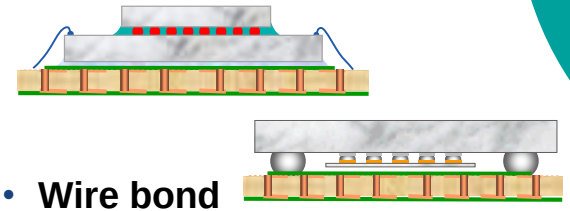
Cu Pillar Micro Bump

Wafer Level Process/ CoW

- Known Good Die
- Both MR & TC available

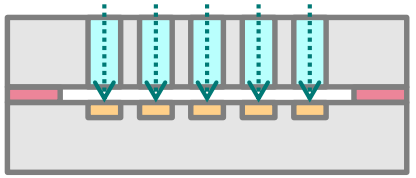
Silicon Photonics

Chip to Board Connection



- Wire bond
- Flip chip (possum)

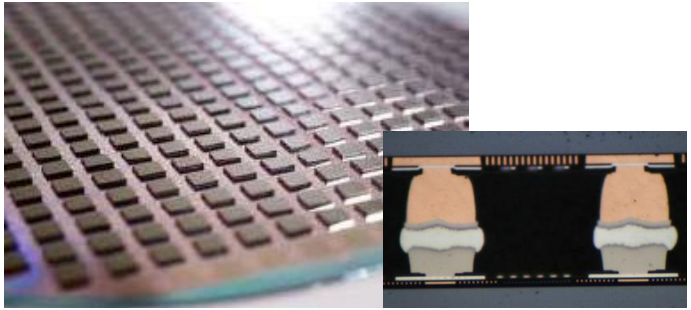
Optical Coupling

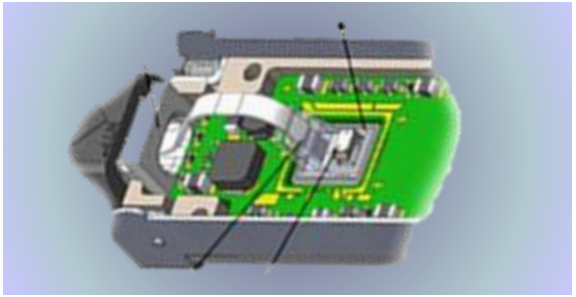


- Various customized design
- Control for alignment

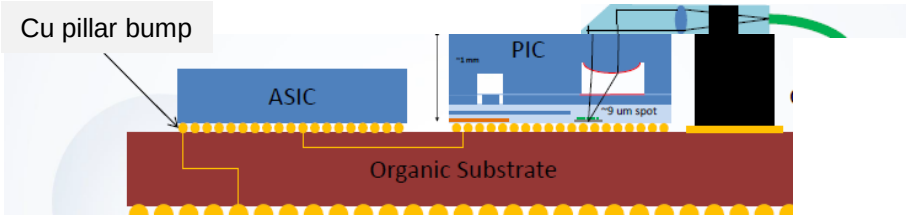
Technologies for Photonics

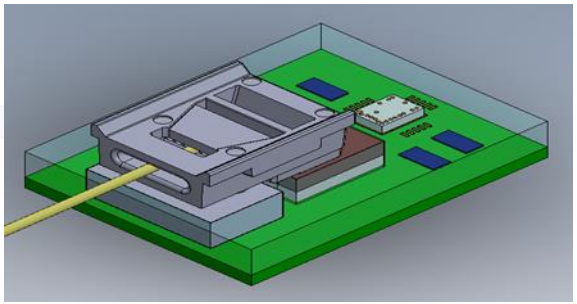
Chip on wafer technology





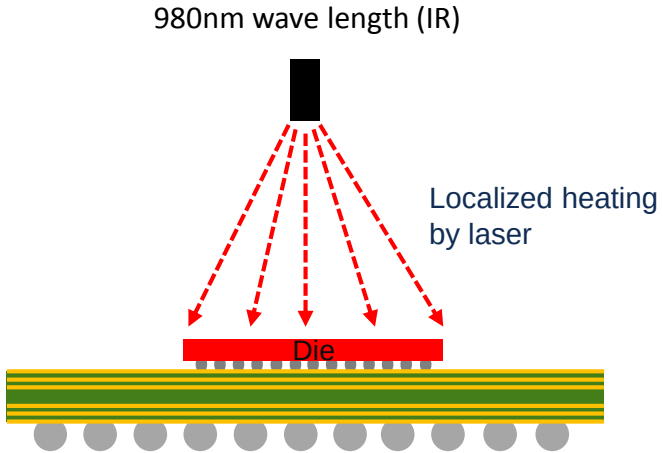
System in Package technology



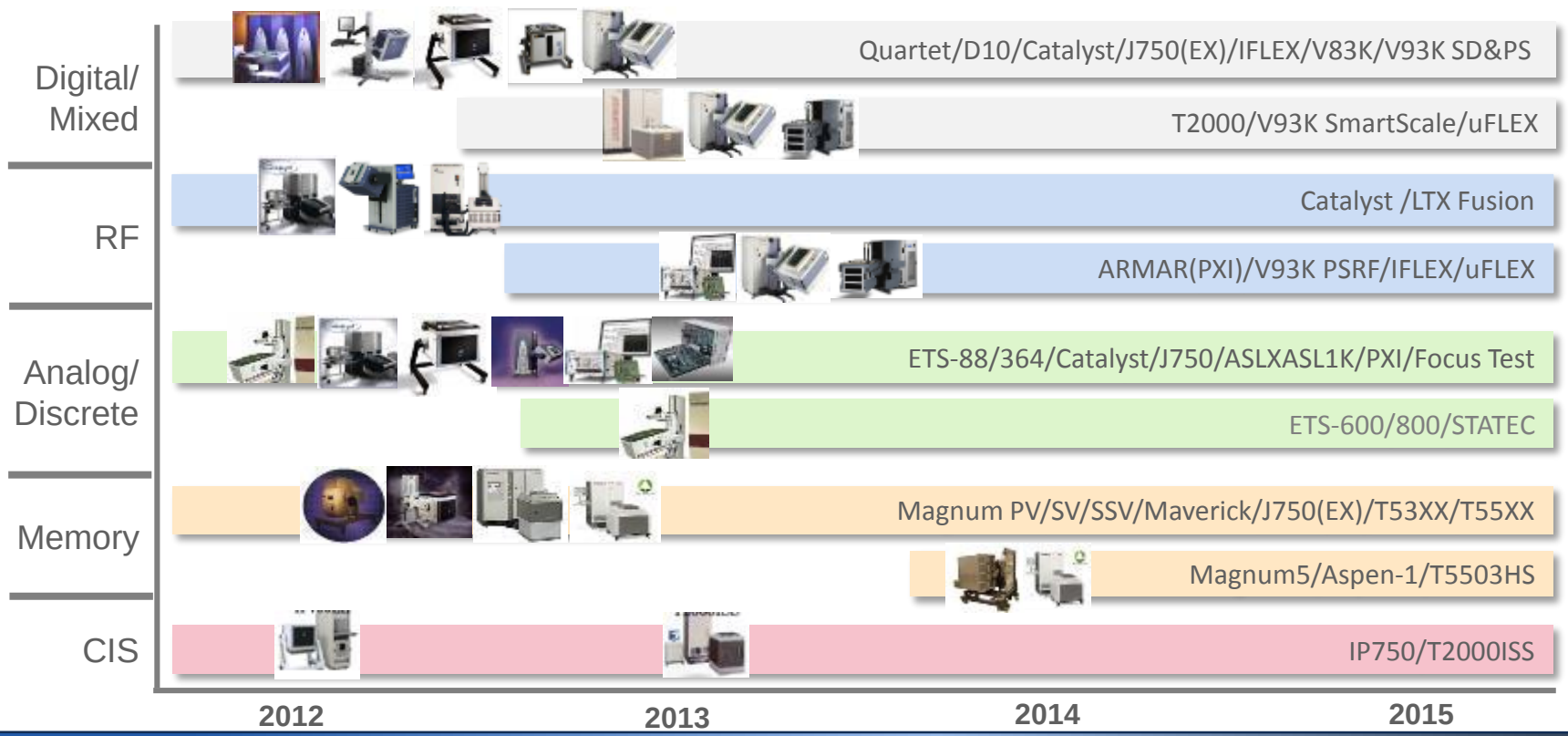


LAB (Laser Assisted Bonding) Technology for lower stress attach

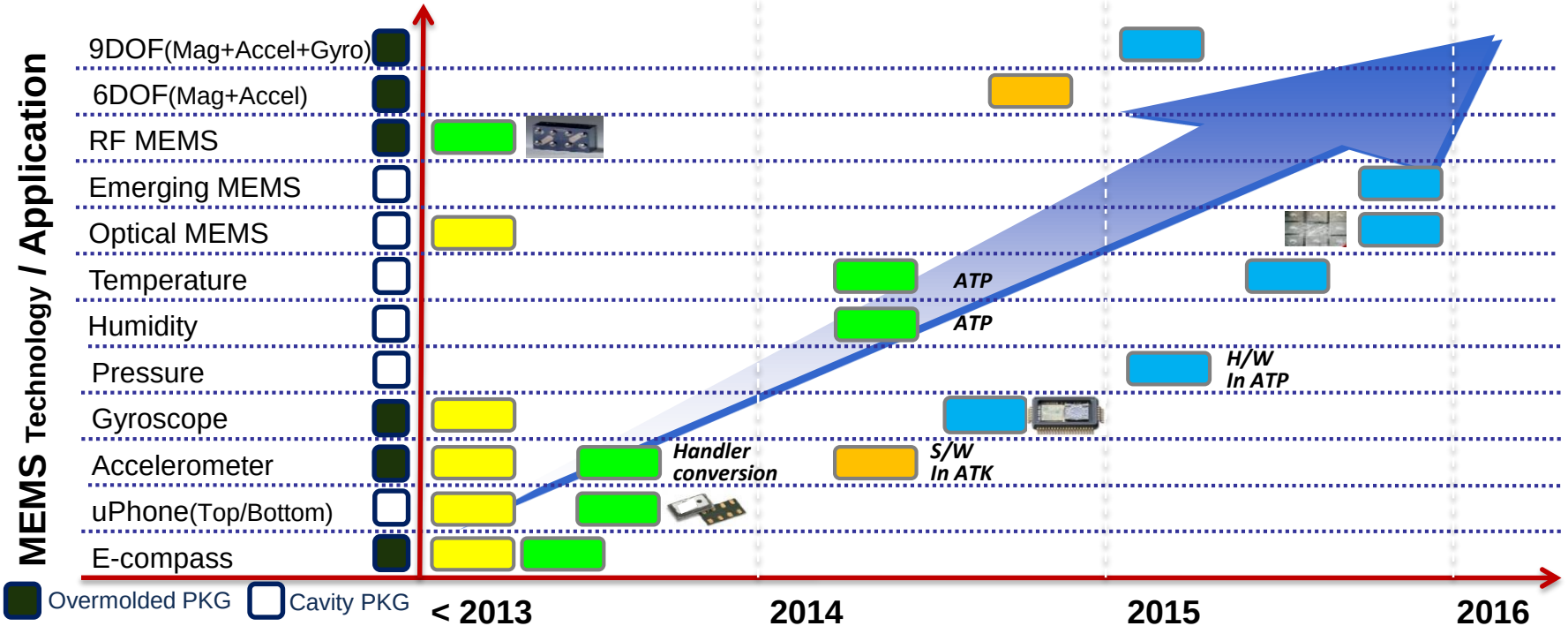
- **New interconnection solution using laser beam after F/C bonding**
  - Only die heat up with area laser (Local reflow concept)
    - Low thermal stress between PCB and die
  - Fast solder melting : High UPH (Same as mass reflow)
- **Target markets**
  - Mobile, networking, consumer, CPU/GPU
  - BB, AP, logic, ASIC
  - Low K device (28nm, 20nm, 14/16nm)
- **Technology advantage**
  - Cost effective process
  - Lower thermal stress than mass reflow



Amkor Tester Availability



Amkor MEMS Tester Development



Global ECO- Society System