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Alpha7L

SoC Tester Overview

Product Background

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◆ Product name

SoC Tester Alpha7L

◆ Features

With test pattern generator which has both properties, logic test pattern generator and memory tester one, the flexible test is possible. And multi measurement is possible.

◆ Electrical Specifications

Fast Digital I/O pin

Per-pin Architecture 100MHz max

VIH/L, VOH/L, IOH/L, VT, PMU, Timing, and so on

TMU : 4 per IO board, 250MHz

◆ Number of fast digital I/O pins

1,024 pins standard (2,048 pins is possible)

◆ Infrastructure Specification

consumption electric power：5KVA（220V single phase）

Size 679(H)×720(W)×800(D) mm

（Main body only : Cable excludes）

Weight About 250kg

size of Rack for PC: 740 (H)×600 (W) ×700 (D) mm

weight: about 70Kg

air: pressure MAX 0.6Mpa amount 50L/Min

Alpha7L Overview

All the tester functions are consolidated in the test head.
（PC and the power supply box are set up in another ）

Prober Docking

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Docking with UF3000

Docking with UF200

Un-Docking

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Specification of Tester

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ITEMS		Alpha7L
Frequency (Period Resolution)		50MHz / 100MHz (500ps / 250ps)
PINS		64 pins per IO board
Multi DUT test		256
Controller		Main CPU and Sub-CPU (The realized reduction the test time in the sub-CPU)
Timing Edge		4 Edge
Timing Group		32
Clock Resolution	TGROUP 0	100 ps
	Except TGROUP 0	1.0 ns
Timing Skew		± 500 ps
Timing Dead Zone		NA
Test Pin Configurations Par pin set	VIH	- 1.45 V ~ + 6.50 V , Hi Volt mode 13 V (1 MHz)
	VIL	- 1.50 V ~ + 6.45 V
	Amplitude	0.05 V ~ 8.00 VP-P
	VOH, VOL	- 1.5 V ~ + 6.5 V (Dual Comparator)
	Termination mode	50 ohm
	Active Load IOH/IOL	0 ~ ± 20 mA
DC Configurations	PMU per PIN	- 1.5 V ~ + 6.5 V, ± 30 mA (PMU/ Pin)
	DPS	8 channel per IO board
LPG Pattern Length		32M / 50MHz , 42M / 100MHz, option to 128M
Instructions		16 Logic Pattern Generation Instruction
		16 Memory Pattern Generation Instruction(option)
ALPG, Data Generation (Option)		4 G x 64 I/O (X16, Y16, Z8), NOR & NAND supported
AD/DA (Option)		AWG 16bit/50KHz, Digitizer 16bit/250KHz
ROM Pattern Memory (Option)		4K x 64bit
Subroutine Pattem Memory		2 K Vector
Buffer Memory (Writing data memory)		1 K Vector
Fail Memory		8K Record
Fail bit Counter		1-set/ 1pin(1024pin system has 1024-set)
Measure Frequency and Time Period		4ch per IO board. 250MHz
Relay Control		64 pins per IO board

Feature 1 ◆Pin Electronics on per-pin method

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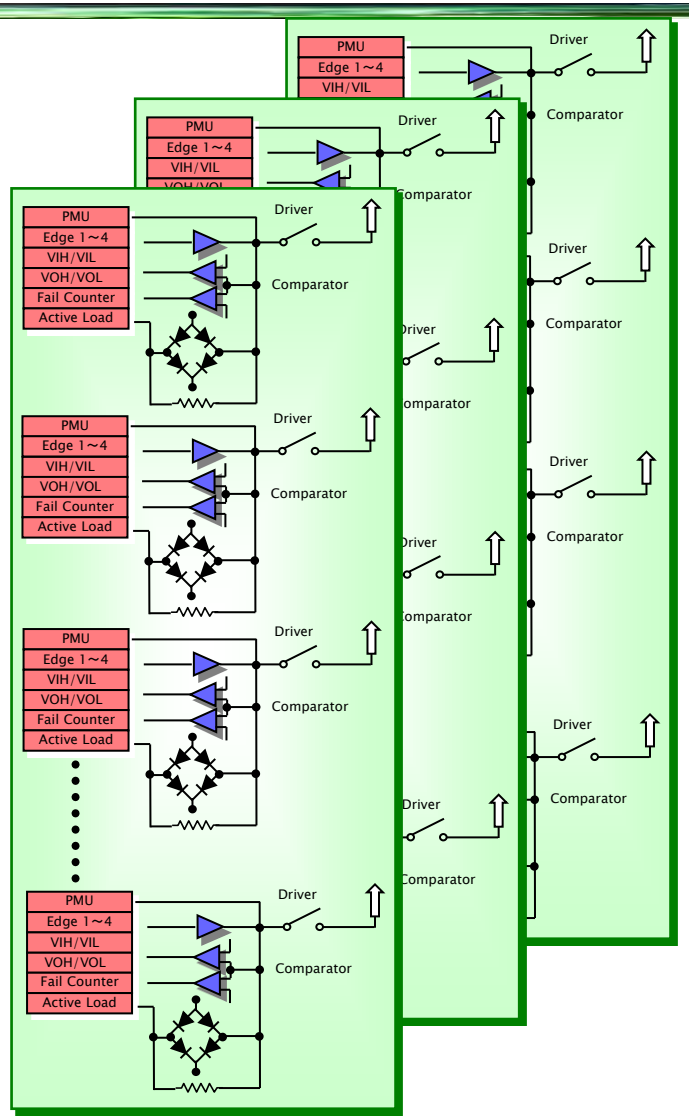
Per-pin Structure (The following functions are loaded at each pin.)

- PMU (High speed DC test is realized.)
- 4 Edge Generator (5bit/vector control)
- VIH,VIL (Changeable at each pin)
- VOH,VOL (Changeable at each pin)
- IOH,IOL (Changeable at each pin)
- Active Load
- 50Ω Terminal
- Relay Control



Feature 2

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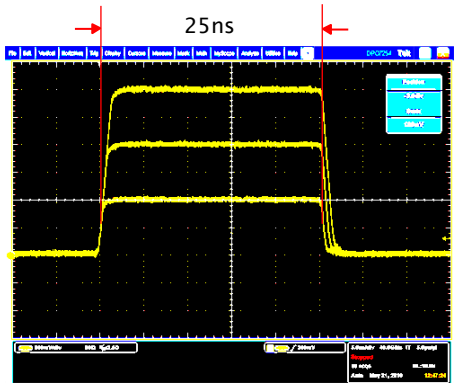
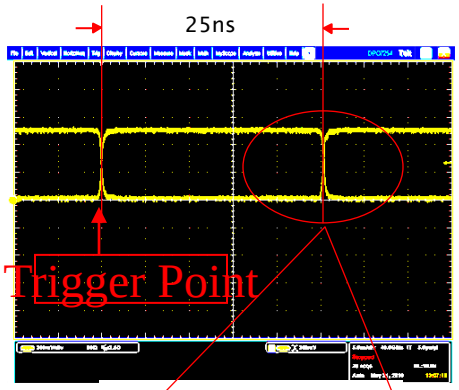
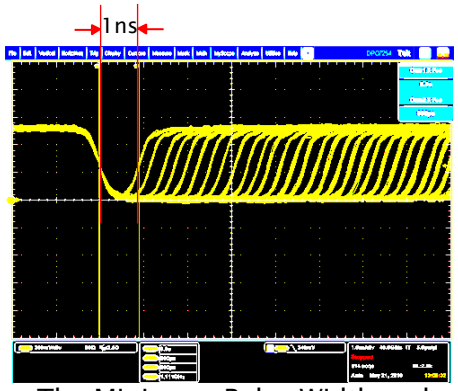
- ◆ Having the capacity of generating the pattern of 100MHz(200Mbps) and 1Gbps as option.
  (Skew±50ps with Paired pin)
- ◆Pulse Drive with low amplitude and high amplitude under 13V Drive are possible.
- ◆Low Jitter design(100ps)



Driver Waveform at every Amplitude
(Setting of Output Voltage:0V-2V, 4V, 6V)

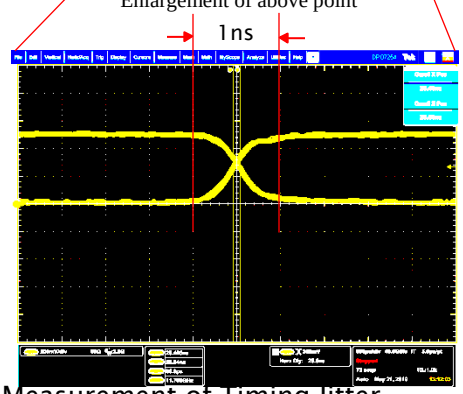


Measurement of Timing Jitter
(Setting of Output Voltage :0V-1.0V)



The Minimum Pulse Width and Timing Linearity
(Setting of Output Voltage:0V-1.0V)
Delay Tap : 250psec

Enlargement of above point



Measurement of Timing Jitter at the next period
(Trigger Point : Last Period)

Feature 3

- The processing speed is raised with built-in distributed processor with every 64ch.
- The great many test at one time is possible with the function of parallel test to large number.

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The function of distributed processor

1. Being high-speed in setting the test condition（Process time is shorten for about 5～10%）
   The host PC does not perform the set a large number of timing, voltage, and current. It is performed with dispersed processor located on every measurement boards.

2. DC test process（Process time is shorten for about 5～10%）
   DC test process at logic I/O pin is performed with dispersed processor.

3. IDDQ test process（Process time is shorten for about 5～10%）
   The dispersed processor makes a role with processing the histogram of IDDQ value, average, and detecting the maximum value and the minimum one.

4. Processing when all numbers are measured at the same time.

Alpha7L Advanced architecture ATE

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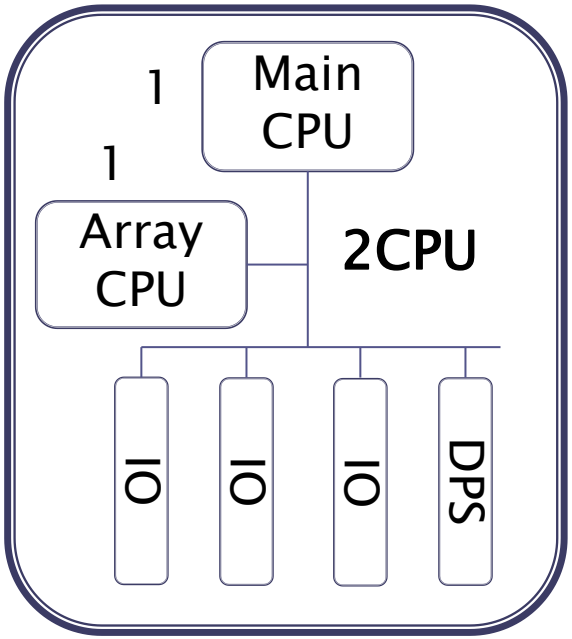
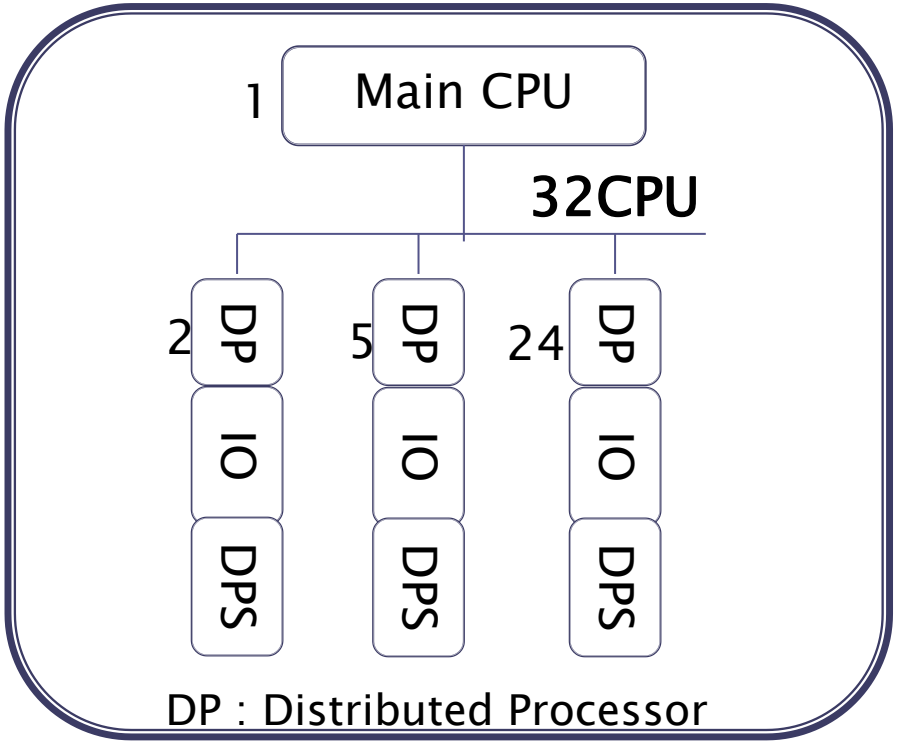
Traditional Tester



Alpha7L advanced Architecture



Feature 4

- Achieved the flexible pin architecture to 1,024 pins.
- Because both functions, LPG(Logic Pattern Generator) and ALPG(Memory Pattern Generator), are loaded, the 1 Pass test is possible.
- Possible to work independently LPG, ALPG and Period Timing with every from 64pins to 1,024pins.

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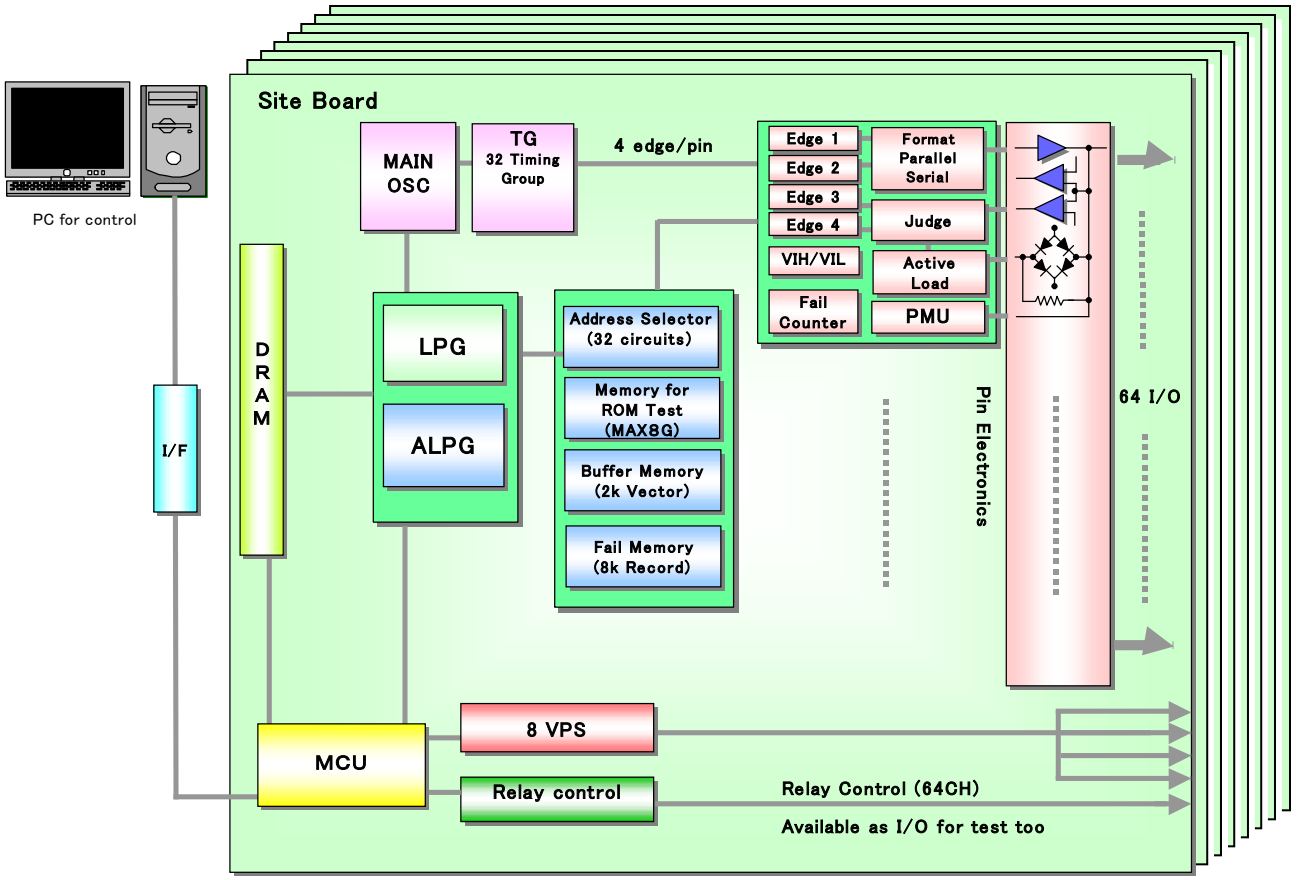

Feature 5

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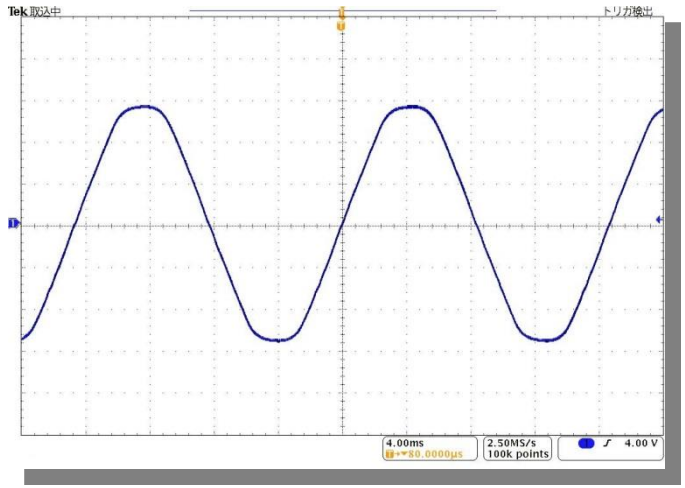
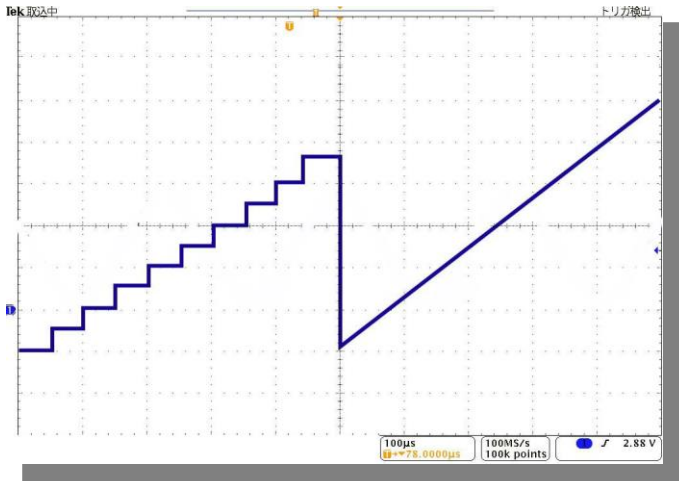
◆Equipped AWG and DGTZ with multi-channels.
（It is possible to change for 4 VPS in 8 ones located in every 64 pins to AWG or DGTZ.）
(Under 1024 pins system ,it is possible to equip 128 channels in the max.)

The function of AWG (50Kbps)and that of DGTZ are loaded.(250Kbps)





Feature 6

◆Designed with high accurate Timing
(Skew between pins ±300ps)

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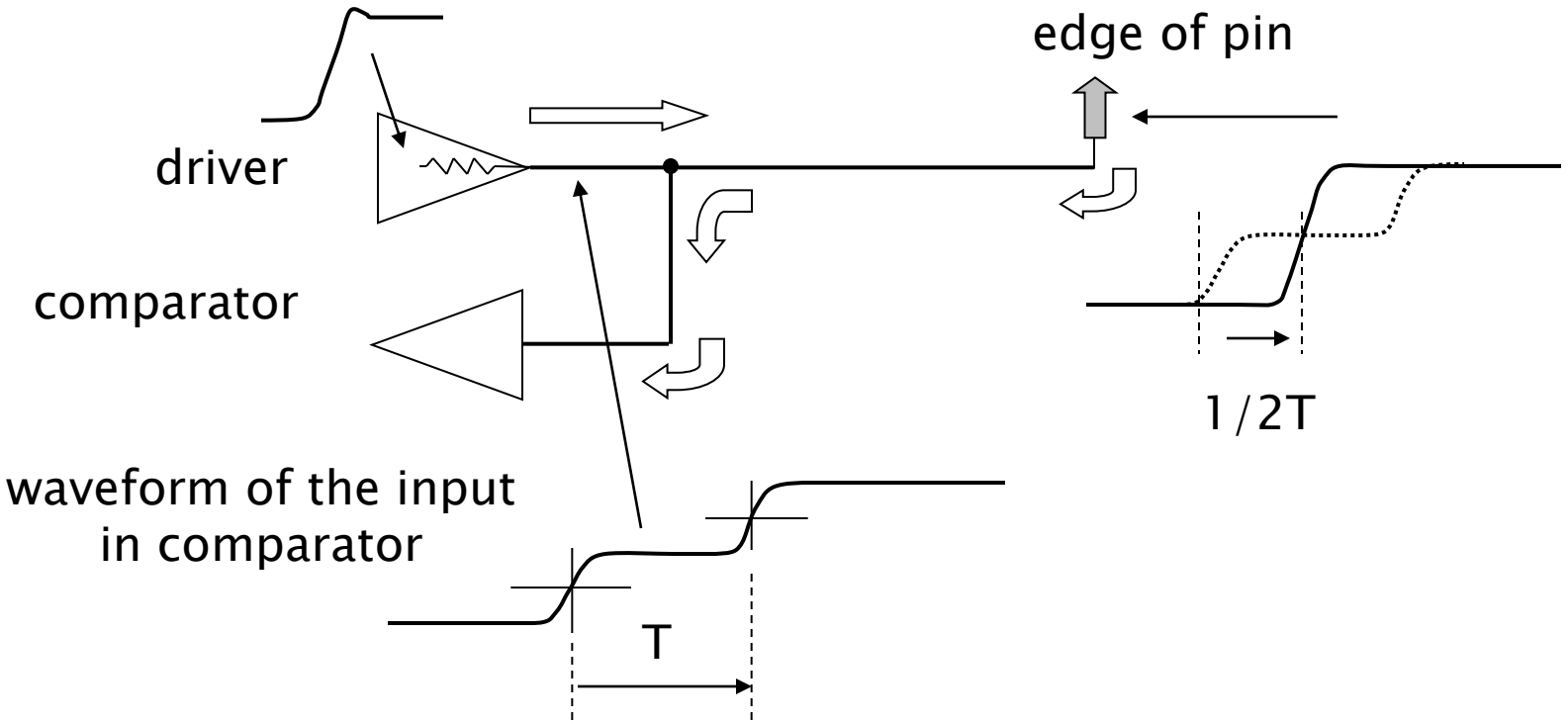
By TDR(Time Domain Reflection) timing measurement method, the timing adjustment at the edge of test cable is realized.



The time from driver to edge of pin detects by TDR measurement.
And the half of this is the time to the edge of pin.

Feature 7

◆ We achieved low cable capacity, 60pF, by being wired in the shortest.

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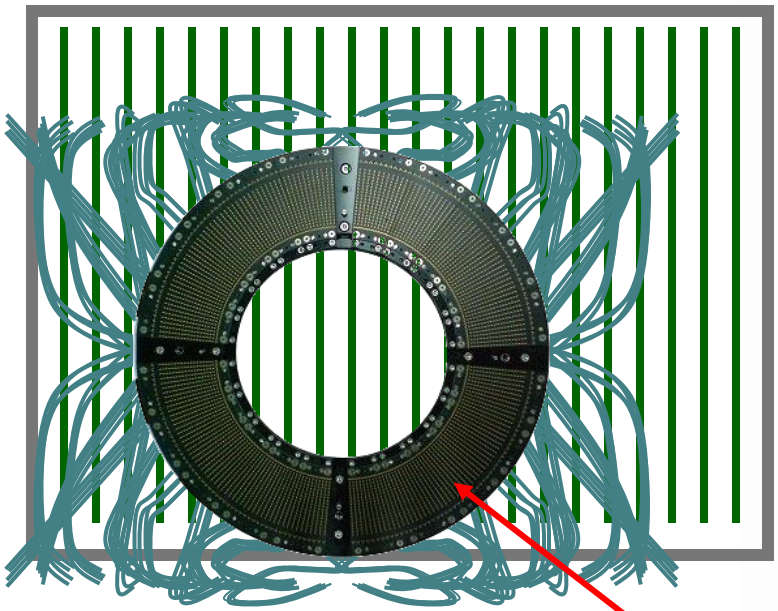
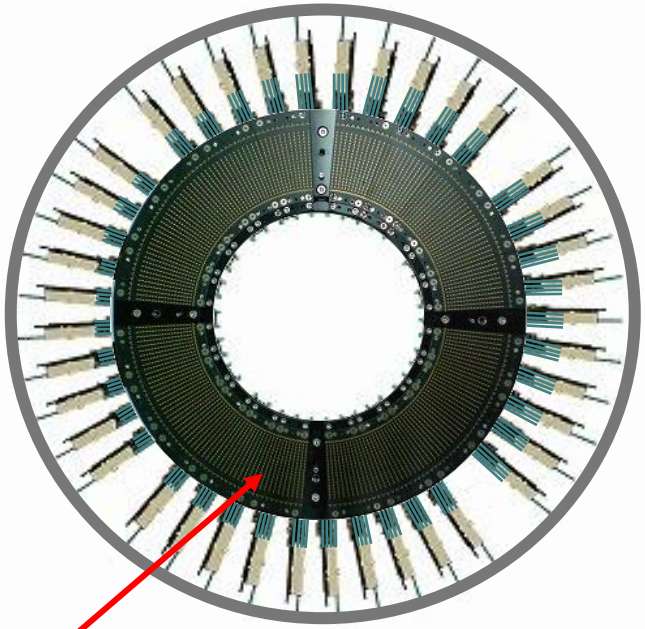
The tester board is located roundly, and wire length to probe card is Shortest (59cm). From this method, the transmitting quality of signal is improved (speed-up of judge).

Other maker's test head



The board location of test head in Alpha7L



Micro-Pin Tower

Feature 8

◆ A low consumption power is achieved
The an annual cost is greatly saved.
◆ Making to low space is achieved(No footprint design).

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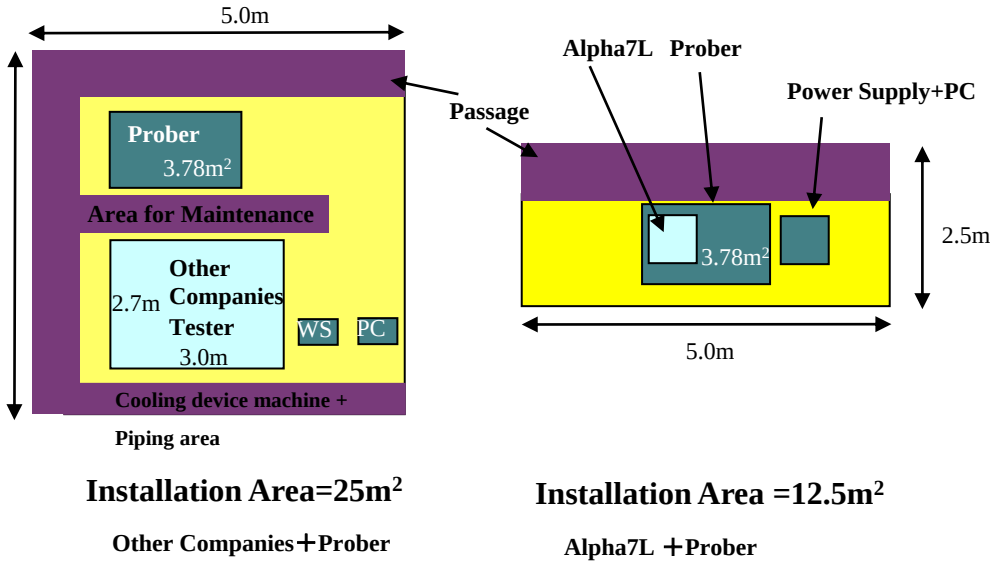
The installation area and power consumption are reduced much more than other makers.
Because the board is equipped with all tester functions.

◆ The annual electricity power cost is reduced for
3 million yen compared with the other companies. (1,024 pins)

Differential annual electric power cost : 10KVA × 22yen/hour × 24hours × 365days ≒ 2 million yen
Differential annual air conditioning cost : 2 million yen/2 = 1 million yen Total is 3 million yen.

*The difference of electric power with the other companies tester is supposed 10KVA.

◆Installation area is 1/2 compared with other makers.



Installation Area=25m²

Other Companies＋Prober

Installation Area =12.5m²

Alpha7L ＋Prober

Operation Software with usability (part1)

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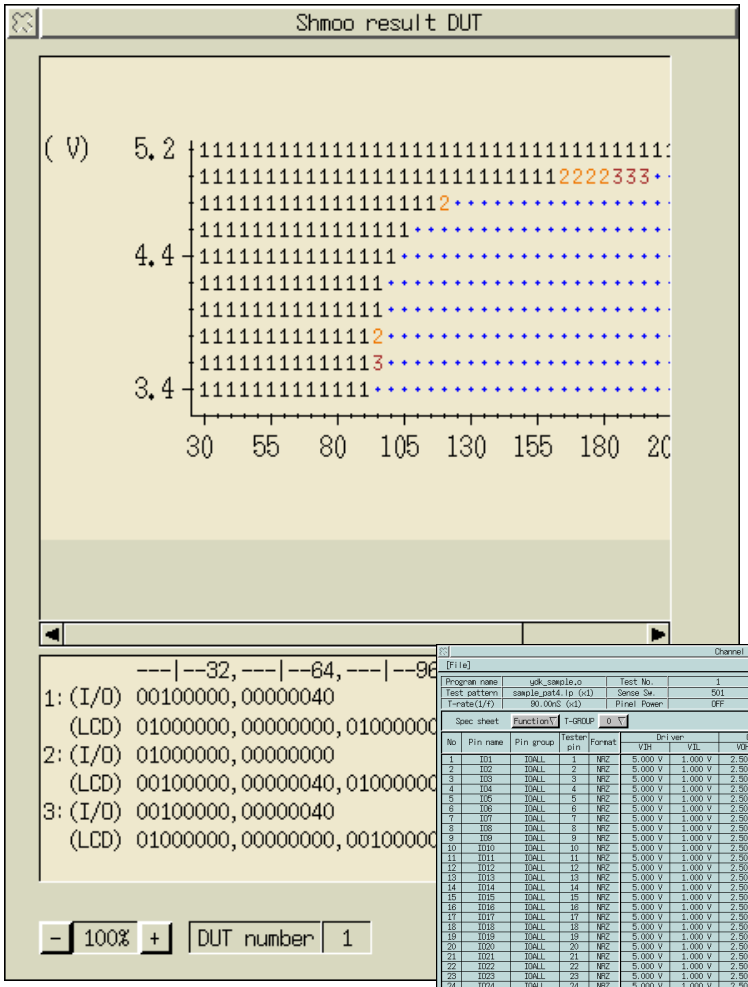
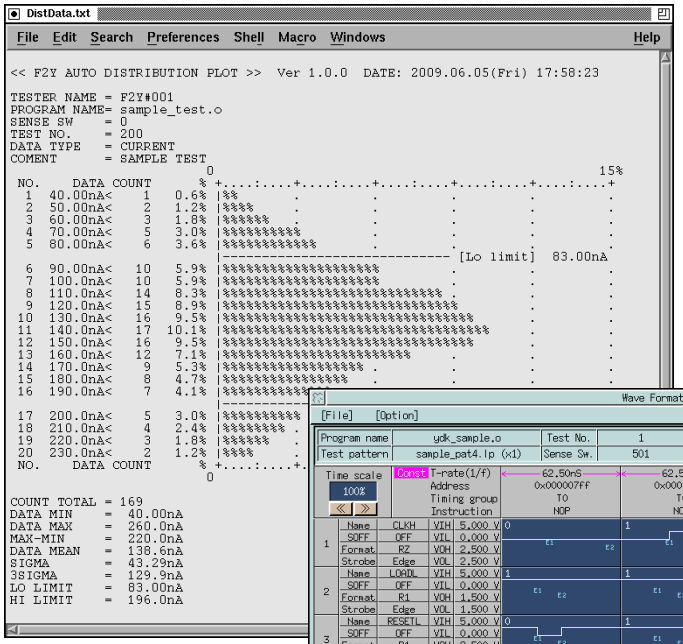
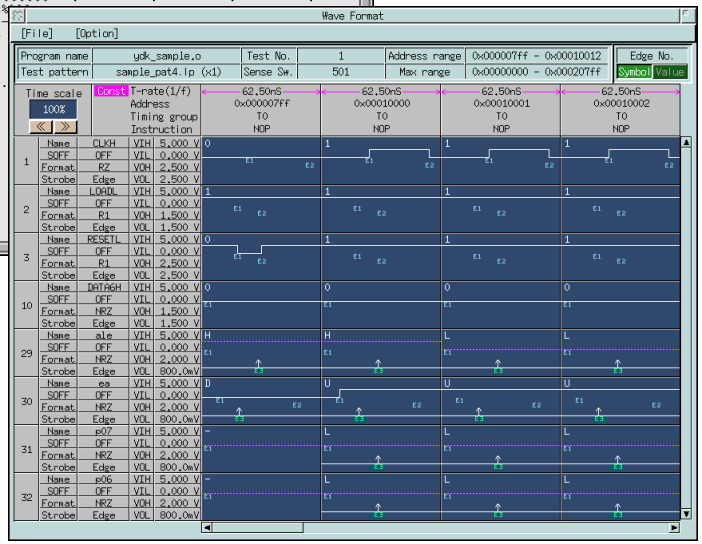


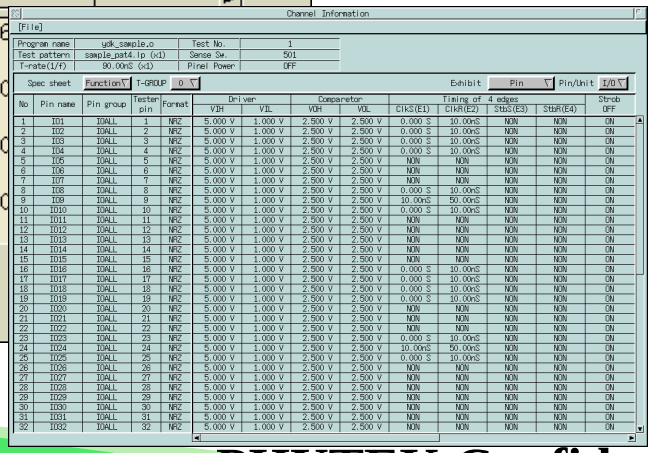
Shmoo Plot



Distribution Plot



Wave Format



Channel Information

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Operation Software with usability (part2)

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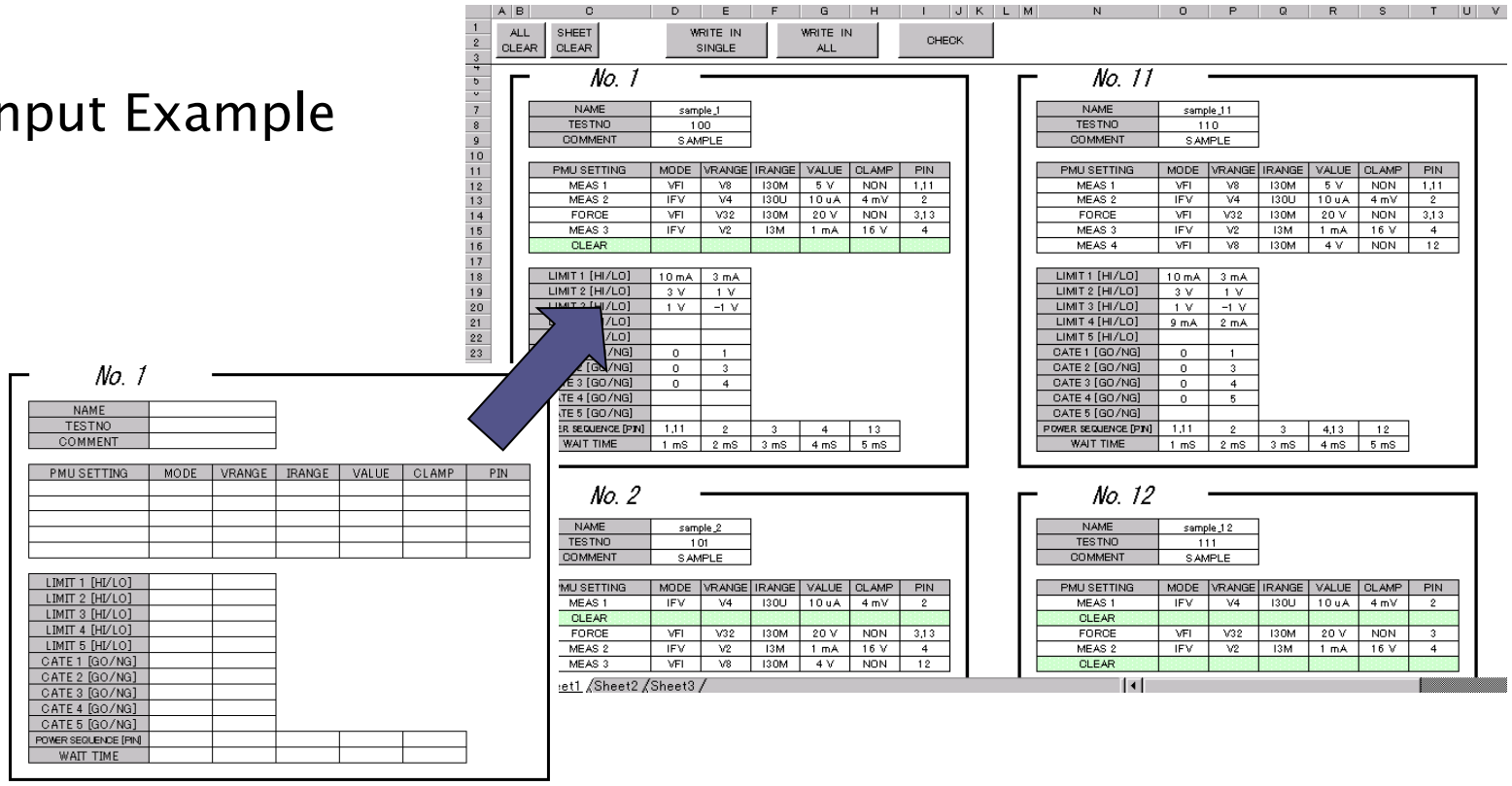
Tool for Test Programming（Option, Developing）
With this tool, it is possible to make a test program easily by Excel input.

＊Input Example



Example of Description in Software (part1)

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Pattern Program Example

```
TPGPROGRAM writetest;
//        00000000 01111111 11122222 22222333
//        12345678 90123456 78901234 56789012


SETADRS(0x0)    // DATA Write

//        D---D--- D---D--- WOC----- CTB------
//        0---1--- 2---3--- EEK----- EEY------

         (00000000 00000000 111----- 11------,T0  C2L 255       XM:=0x00 YM:=0x0  MA )  ←ADRS LOOP COUNT SET
LE0:     (00110111 01010000 111----- 11------,T0  SUB LE0PROG                     MA )  ←DATA WRITE SUBROUTINE

         (00100101 01010110 111----- 11------,T0  C2J LE0                         MA )  ←LOOP JUMP
         (00110011 00000101 111----- 11------,T0  STOP                            MA )  ←PATTERN STOP


LEOPROG:(00000000 00000111 111----- 10------,T0  C1L 600                         MA )  ←MAC COUNTER SET
         (00000000 00000111 111----- 10------,T0  BUF                             MA )  ←LPG DATA STORE
         (01110111 01110111 111----- 00------,T0  NGD         YR:=0xAA XR:=0xAA   MA )  ←NG DISABLE
         (MBBBMBBB MBBBMBBB 010----- 00------,T0  SIFT 4      YR:=0xAA XR:=0x55   RA )  ←CODE AAAA OUTPUT
         (MBBBMBBB MBBBMBBB 010----- 00------,T0  SIFT 4      YR:=0x55 XR:=0xAA   RA )  ←CODE AA55 OUTPUT
         (MBBBMBBB MBBBMBBB 010----- 00------,T0  SIFT 4      YR:=0xAA XR:=0x5A   RA )  ←CODE 55AA OUTPUT
         (MBBBMBBB MBBBMBBB 010----- 00------,T0  SIFT 4                          RA )  ←CODE AA5A OUTPUT
         (MBBBMBBB MBBBMBBB 010----- 00------,T0  NOP                             MA )  ←ALPG DATA OUTPUT
         (00000000 00000000 110----- 00------,T0  NOP                             MA )
LE:      (H000H000 H000H000 101----- 00H-----,T1  MAC LE                          MA )  ←STATUS CHECK
         (-000-000 -000-000 101----- 00------,T0  NGE                             MA )
         (P000P000 P000P000 100----- 00------,T0  NOP          XM+1 L+1           MA )  ←DATA CHECK
         (01110111 01110111 111----- 00------,T0  RET                             MA )  ←SUB ROUTINE RETUEN
END.
```

Example of Description in Software (part2)

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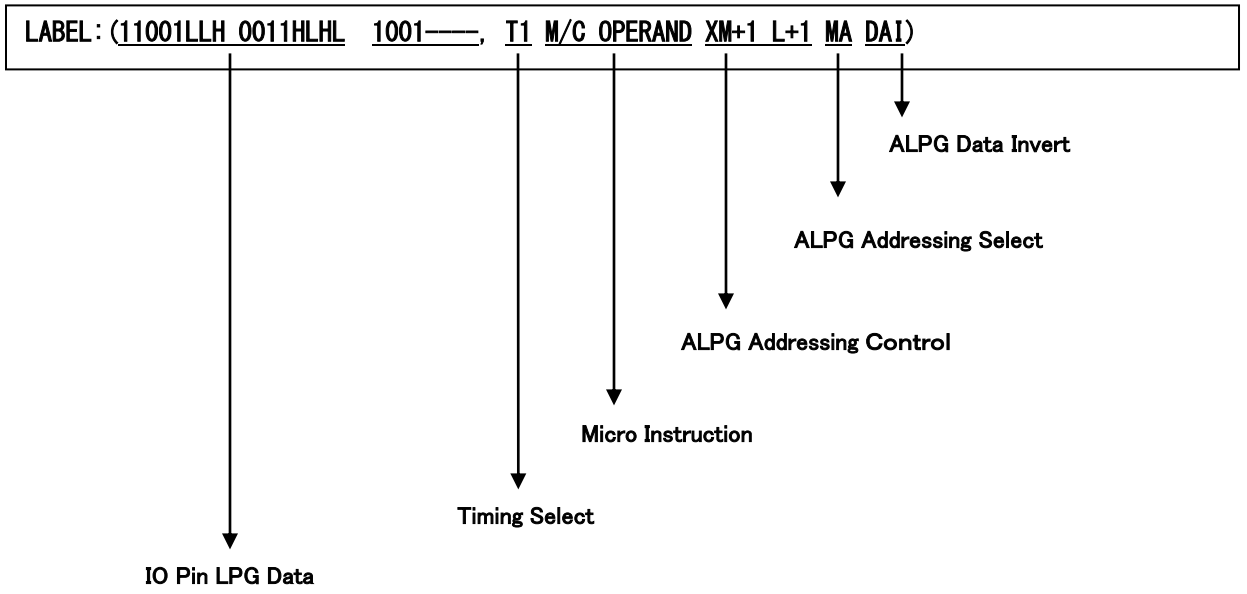
Pattern Program Format



Label :	Pattern Code at driver	Timing Select	Micro Instruction			Operand	ALPG Control	ALPG Output Select	ALPG Data Invert
	PIN1,2,3,..	T0～T15	NOP	CFJ2	M/B	M:=B	L±	MA	DAI
			JMP	MAC	M/C	B:=M	M:=	MI	
	0, 1		SUB	CFC	M/R	XM:=XB	B:=	BA	
	L,H		RET	C3J	R/C	XB:=XM	R:=	RA	
	D,U		C1L	CFR1	XM/XB	YM:=YB	XM:=	XMA	
	−,=		C2L	CFR2	XM/XC	YB:=YM	YM:=	XMI	
	B,F		C1J	NGD	XM/XR	M±	XB:=	XBA	
	Z		C2J	NGE	XR/XC	R±	YB:=	XRA	
			C3L	LPF0-7	YM/YB	XM±	XR:=	YMA	
			REP	UCSTAR	YM/YC	XR±	YR:=	YMI	
			SIFT	T	YM/YR	YM±		YBA	
			STOP	UCSTOP	YR/YC	YR±		YRA	
			CFJ1						

Customer Reference

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GENUSION

MegaChips

OKI Open up your dreams
OKI Digital Imaging

EPSON
EXCEED YOUR VISION

Panasonic


Thank
You