Smart power technology needs smart substrate

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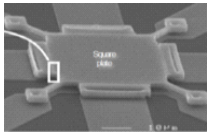
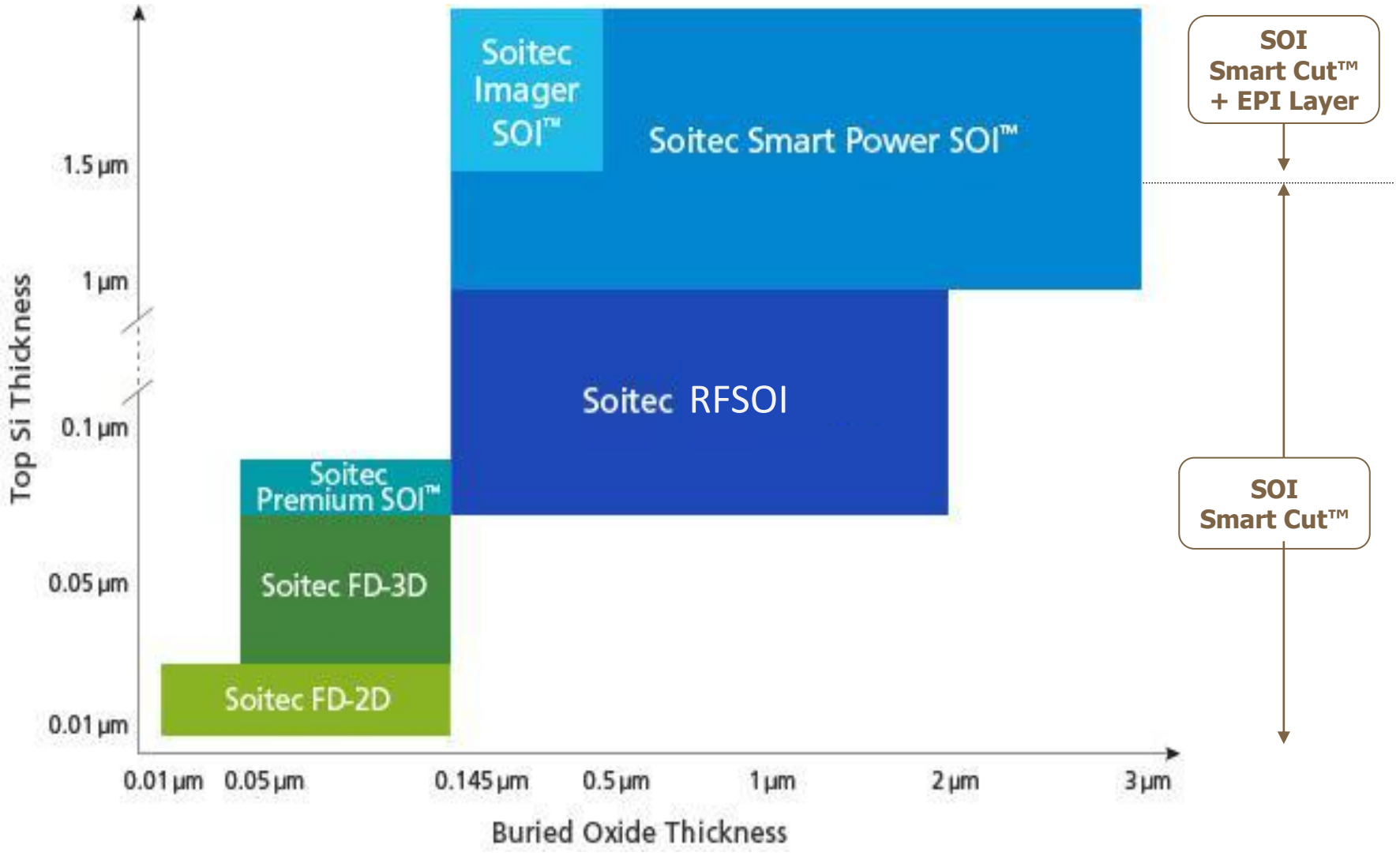
Soitec product portfolio adapted to wide markets

		Applications					
		Digital	**Power / analog**	**RF**	**Image sensors**	**Photonics**	**MEMS**
Markets	**Computing / Infrastructure**						
	Consumer / Mobility						
	Automotive and industrial						
	Soitec products	FD-2D FD-3D Premium SOI	Smart Power SOI	Wave SOI HRSOI- eSI RF SOS	Imager SOI Stacking for Imager	Photonics SOI	Stacking for MEMS

Soitec – Leader in Engineered Substrates



Outline

1. Power market overview
2. BCDMOS and isolation technologies
3. Smart Cut™ SOI: a cost competitive technology
4. Conclusion

Wide range of application & Large market size

Industrial

•$2.5B/15.8%

•Power grid
•Medical
•Home building

Automotive

•$5.6B/3.5%

•Car, truck
•EV/HEV

Communication

•$13.7B/7.6%

•Smart phones, tablets

Consumer

•$3.1B/8%

•Lighting
•White goods

IT

•$4.6B/4.2%

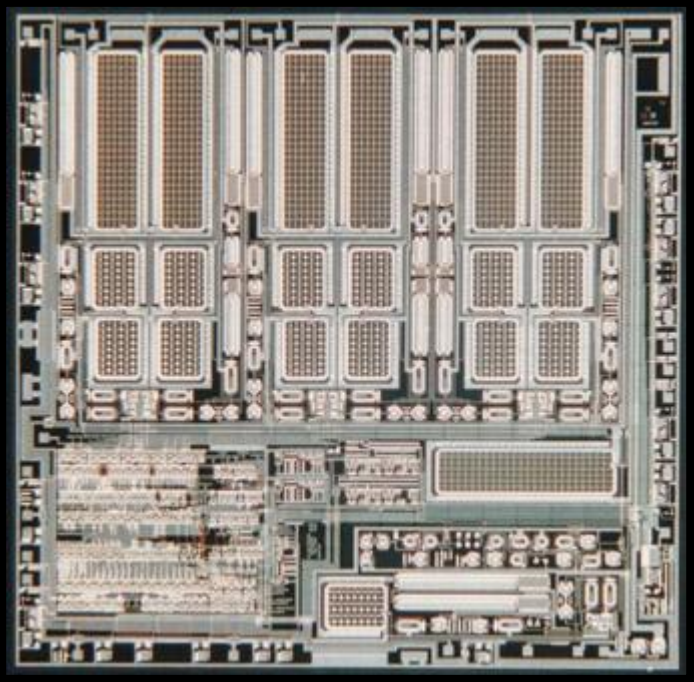
•Desktops
•Fax, printers, scanners
•Servers, NAS

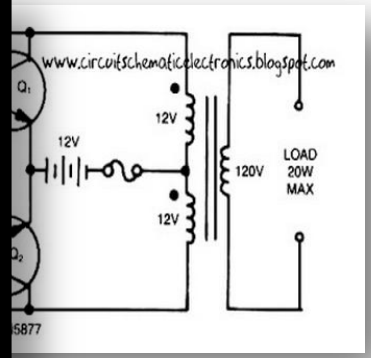
Market size $B / CAGR % (Source: IHS iSupply 2013)

Smart power evolution

Logic function (CMOS)
Smart control
Interface to digit

Basic power function (DMOS)
onversion





NVM Memory
Store state
Smart evolution

Control sensor
Voltage/current overload
Temperature

Integration examples

LED lighting

Driver

- Converting wall power for LED
- Dimming capability
- Remote control (wifi, bluetooth,…)

Communication

AMOLED power supply

- Positive and negative output supply
- Adjustable controlled output
- Thermal overlaod protection

Automotive

Gate driver IC

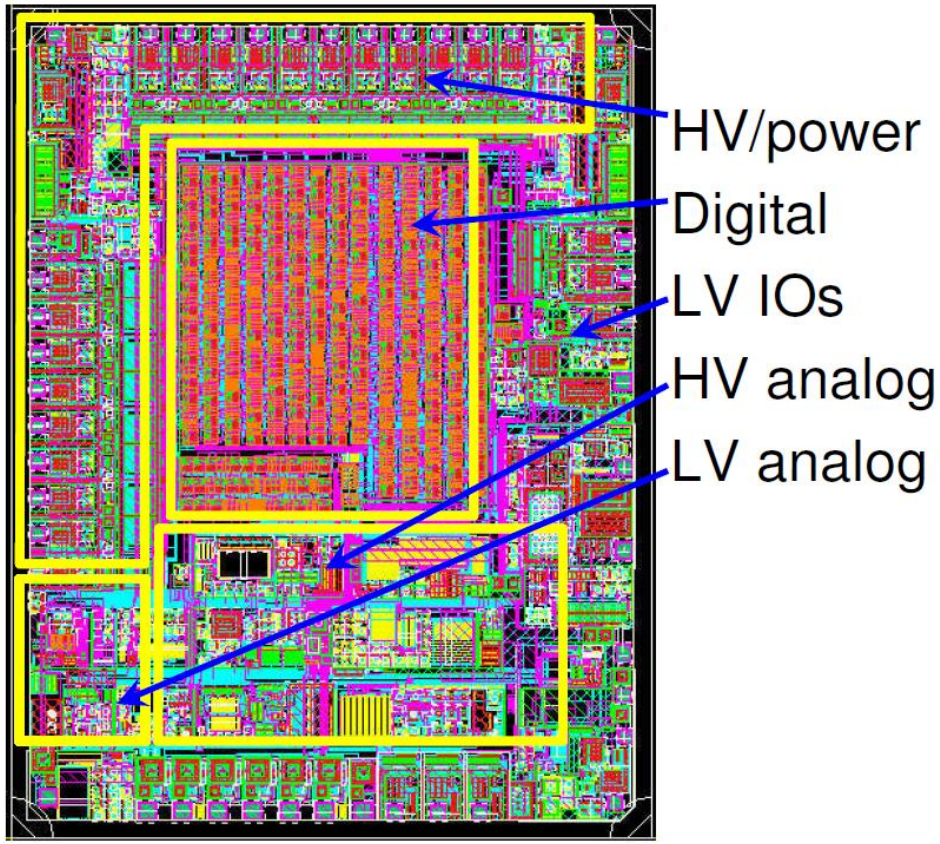
- Gate drivers for fast switches, high efficiency
- IC closer to engine
- Remote controlled

Home building

Power over Ethernet

- Delivery power through ethernet cable
- Large variety of point of load: flexible & configurable DC/DC converter

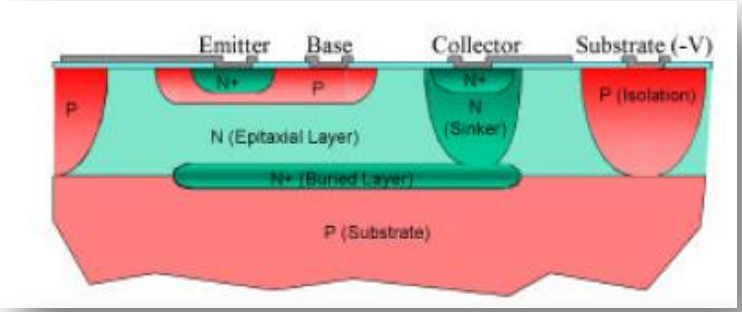
BCDMOS platform for smart power

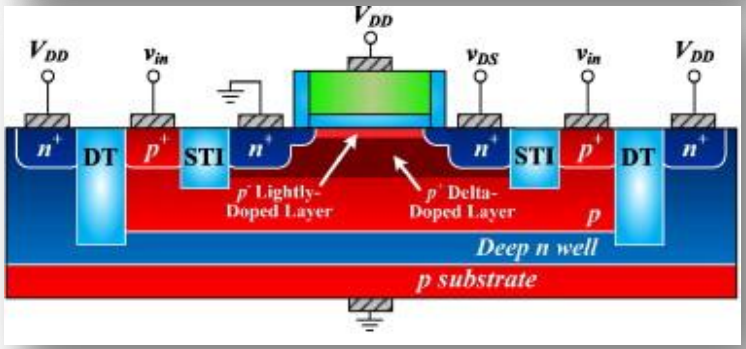


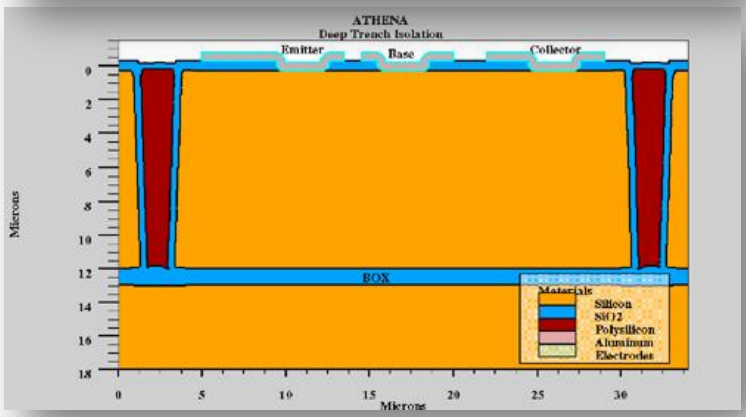
BiPolar + CMOS + DMOS = integration of Analog + logic + power functions
SMART POWER technology

Integration of different voltages

Key process is isolation







PN junction isolation

-Deep implant
-Large guard ring
-Surface penalty

Deep trench isolation and PN junction

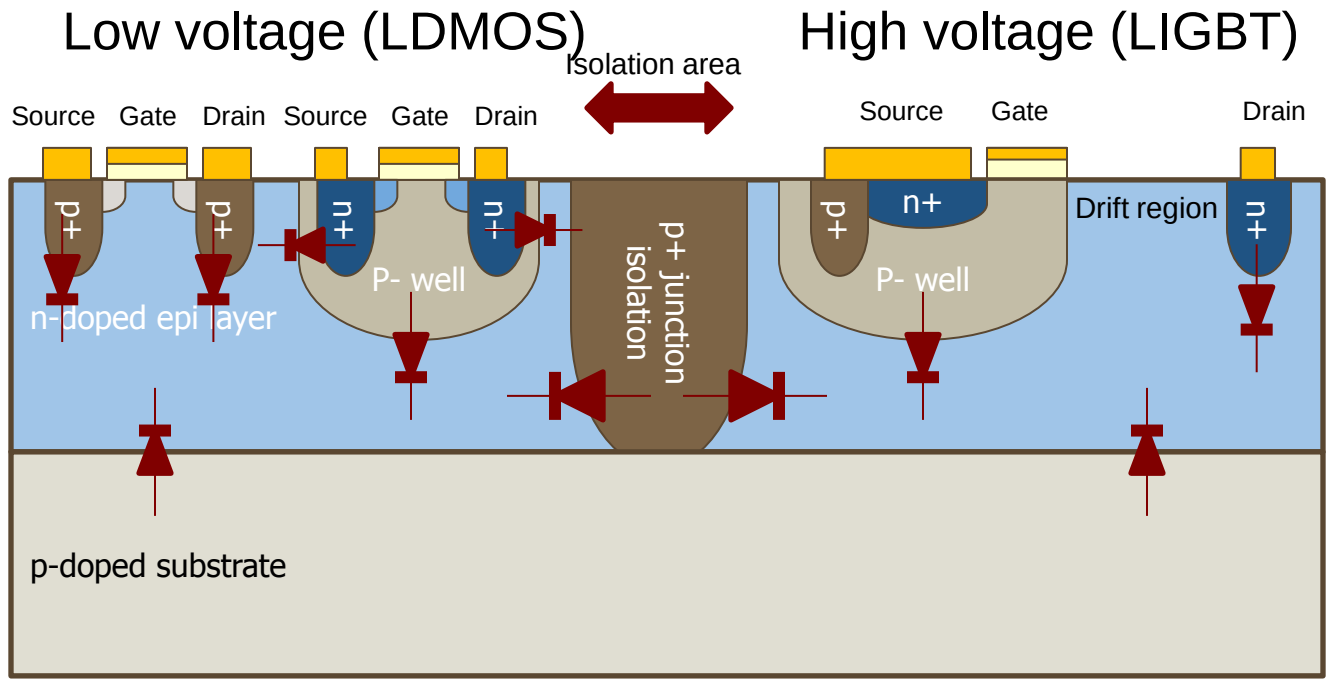
-Deep trench for lateral isolation
-PN junction for vertical isolation
-Reduced surface penalty

Deep trench isolation and SOI

-Full isolation (lateral and vertical)
-Surface saving
-EMI immunity

Bulk low voltage and high voltage integration :

Electric isolation through pn-junctions

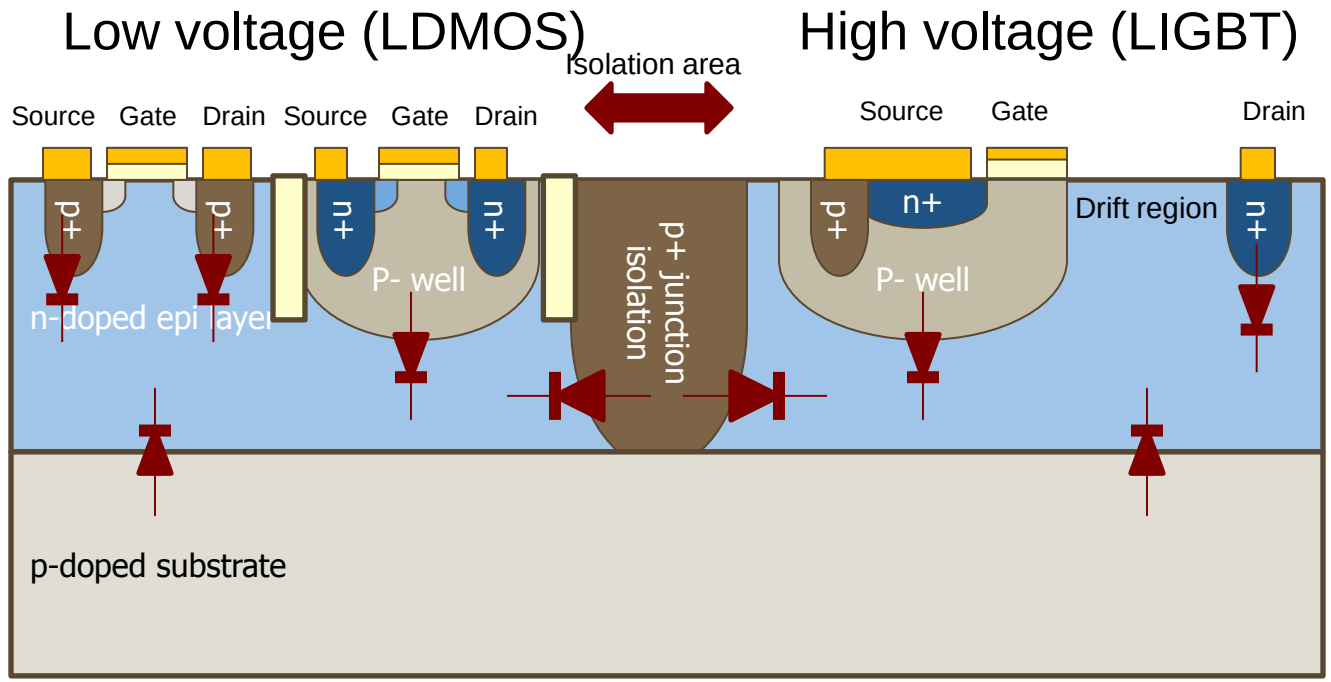


Parasitic pn junction

To isolate low voltage and high voltage areas :
Lateral pn-junction
Vertical pn-junction (impose a p substrate with n-epi layer)

Deep trench isolation :

Electric isolation through dielectric trenches and pn-junctions

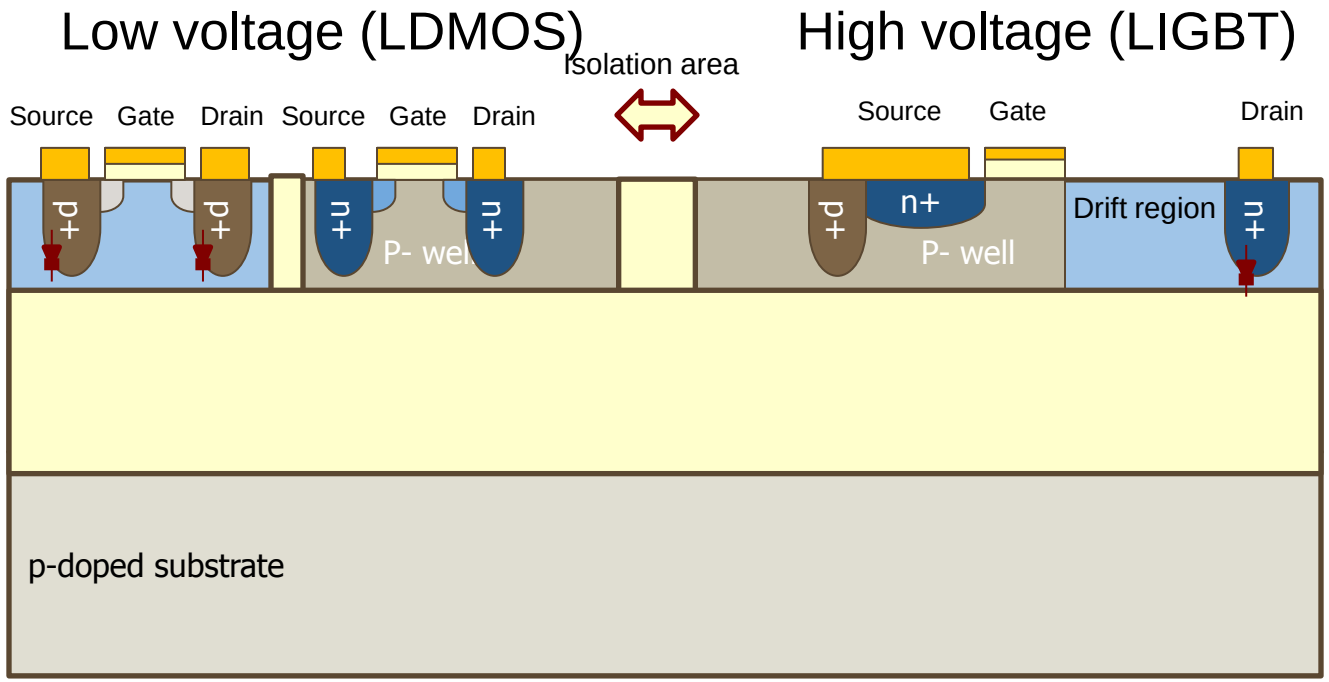


Parasitic pn junction

Increase trench isolation breakdown through voltage divider concept
Vertical pn-junction (impose a p substrate with n-epi layer)

Dielectric isolation benefits :

Silicon island enables different voltage integration



Parasitic pn junction

Remove parasitic pn-junction
Improves leakage performances, thermal range operation

SOI benefit at the device level

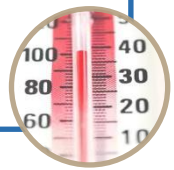
Improvement benefit by categories

No pn junction for p well

No pn junction with substrate

High temperature

Up to 225°C



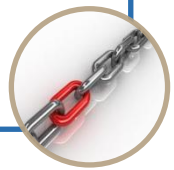
No latch-up

Reduce coss-talk

ESD/EMI immunity

High reliability

Truely free latch-up



Low leakage

High switching frequency

Low Rdson

Performances

Rdson < 1Ω.cm (*)

* Piet Wessels, Migas 2009

Small trench isolation

Easy voltage stacking

Integration

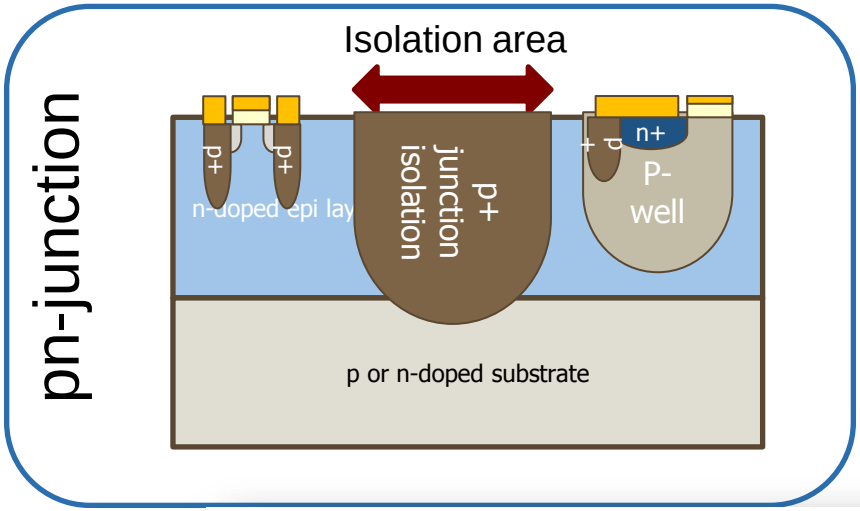
Die shrink ~40%

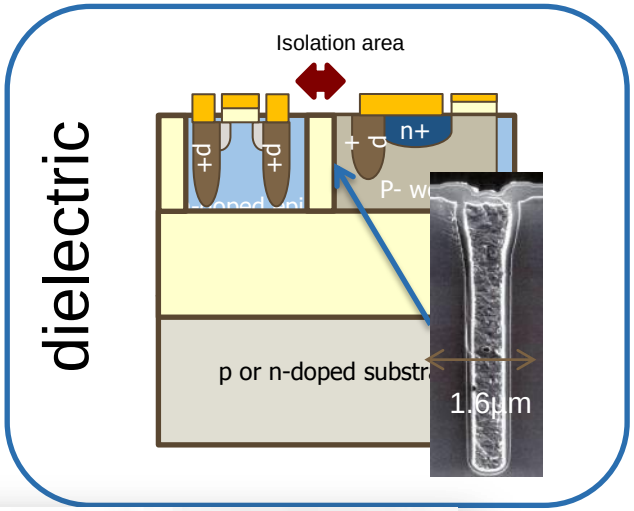
Up to 600V IGBT integration

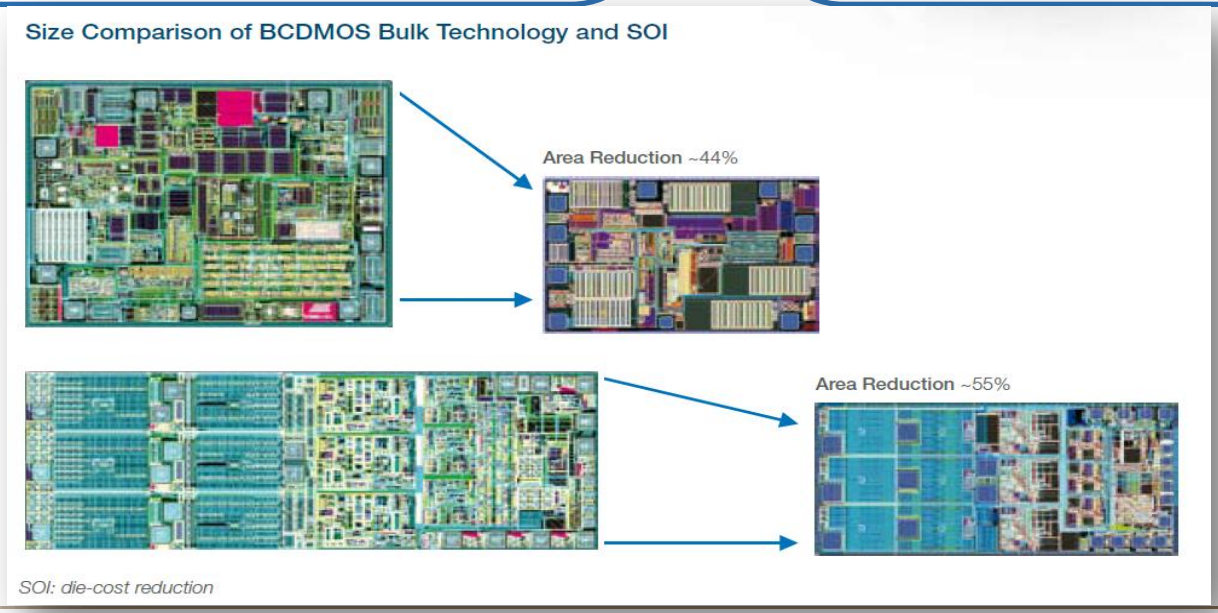
Electrical isolation with substrate

High voltage

Die shrink enables cost effective solution







Courtesy ATMEL

RESURF *(Reduces Surface Field)* Technology

How to guarantee a high Breakdown voltage

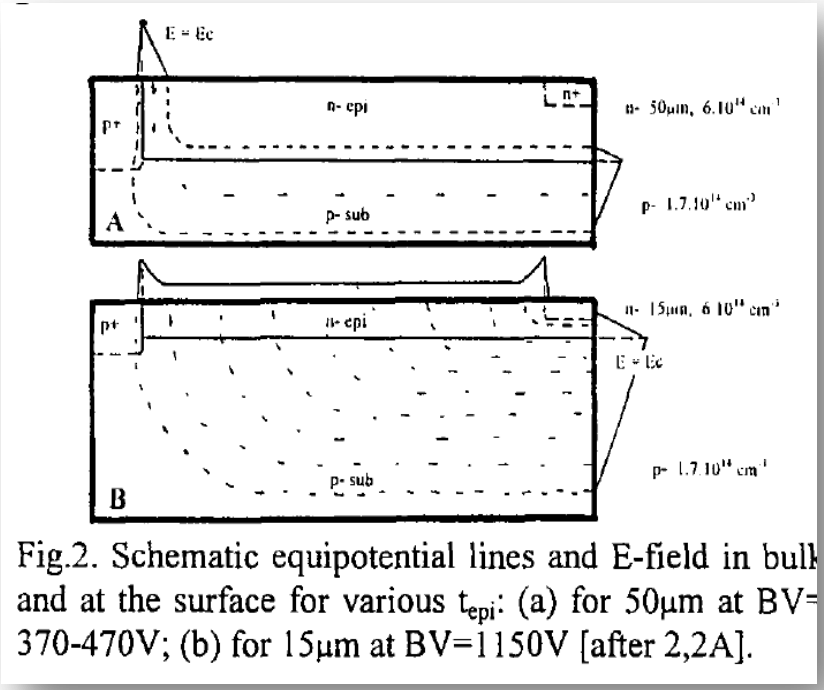
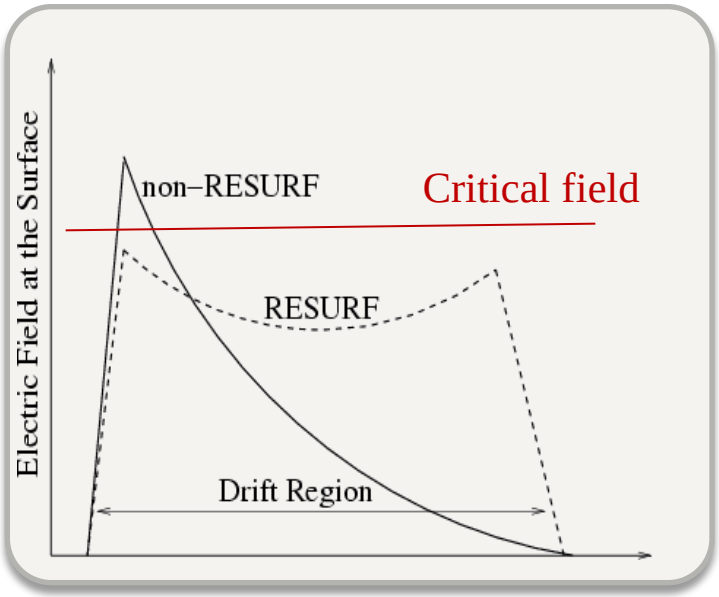


Fig.2. Schematic equipotential lines and E-field in bulk and at the surface for various t_{epi}: (a) for 50µm at BV= 370-470V; (b) for 15µm at BV=1150V [after 2,2A].



Relationship between silicon thickness and doping concentration : to guarantee

electrical field in the drift region ≤ critical field (limit)

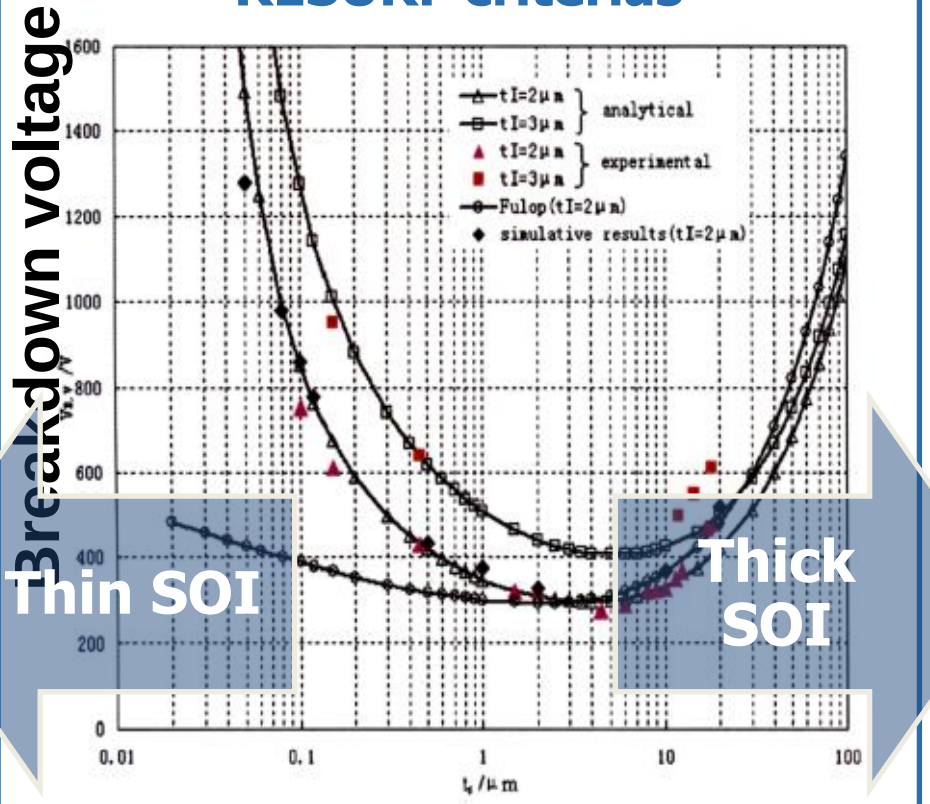
RESURF Technology in SOI

Two options

Option thin SOI

SOI <0.5µm
Uniformity <0.05µm

Thickness conditions to match RESURF criterias



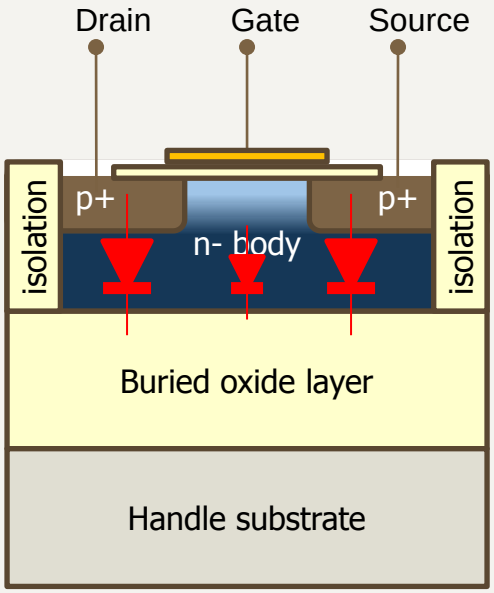
Option thick SOI

SOI >3µm
Uniformity <0.5µm

S. HU & Al, Int. Conf. on Communication, Circuits and Systems, ICCCAS 2008

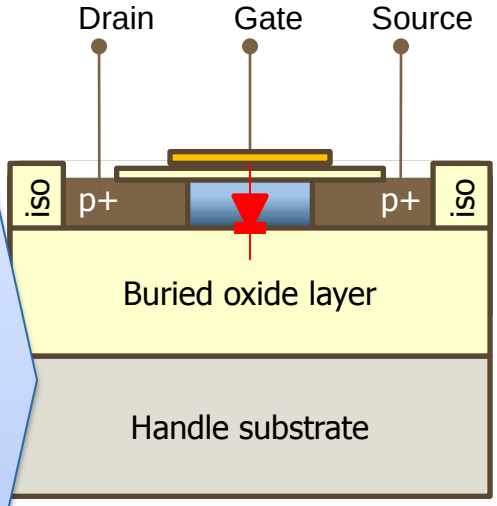
SOI-BCDMOS flavors: *Get more benefit from SOI*

THICK SOI
Bulk like design



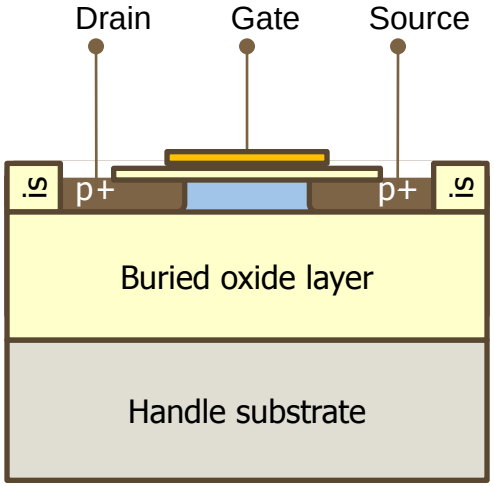
- Dielectric isolation
- 1. Source,drain parasitic junction
  2. Channel parasitic junction

THIN SOI
Partially depleted



- Dielectric isolation
  No source,drain parasitic junction
- Channel parasitic junction

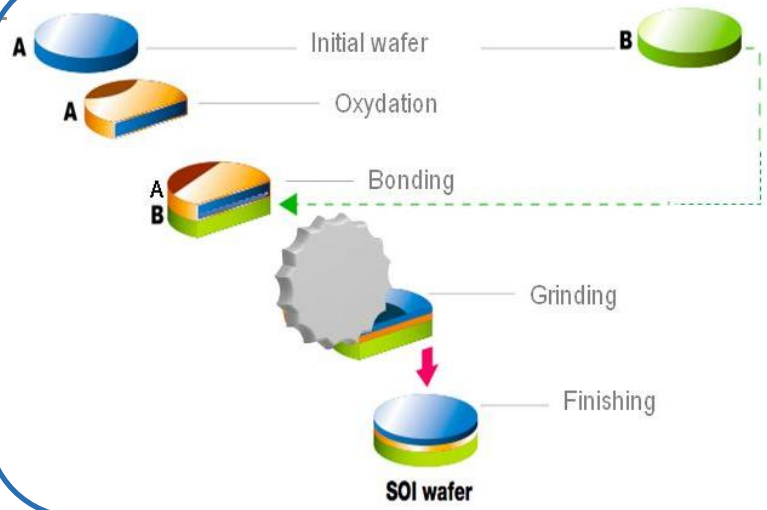
THIN SOI
Fully depleted



- Dielectric isolation
  No source,drain parasitic junction
  No channel parasitic junction

SOI wafer technologies for power

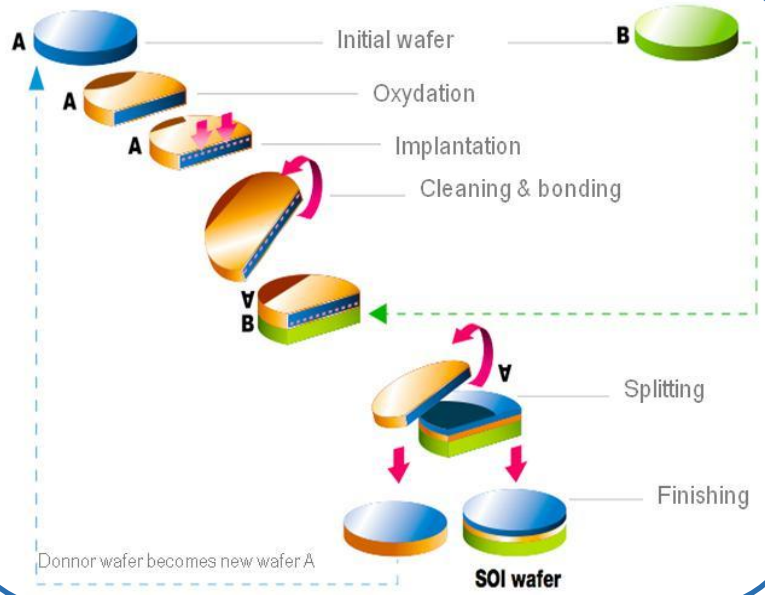
BSOI



Min SOI thickness ~ 3µm
Max SOI thickness ~100s µm
Uniformity ~0.5µm

2 wafers to build 1 SOI

Smart Cut™



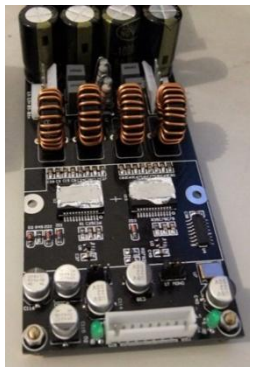
Min SOI thickness ~ 0.1µm
Uniformity ~0.01µm
Max SOI thickness ~few µm

<2 wafers to build 1 SOI

Benefit at chip level and system level

DEVICE

Thin SOI	Thick SOI	Bulk
Optimum RESURF	Non optimal RESURF	Non optimal resurf
High switching speed	Switching speed	Switching speed
Lower Rdson	Small Rdson	Small Rdson
No latch-up	No latch-up	Latch-up
Very smaller devices	Small devices	Large devices
Trench isolation	Deep trench isolation	Junction isolation



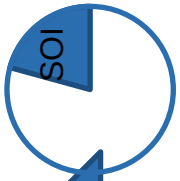
SYSTEM

System size/weight	System size/weight	System size/weight
Total BOM cost	Total BOM cost	Total BOM cost
ESD/EMI protection	ESD/EMI protection	ESD/EMI protection
Medium current	High current	High current

SOI penetration in power market

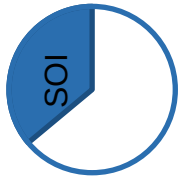
Industrial

- Ultrasound Medical imaging
- Oil drilling
- Aerospace



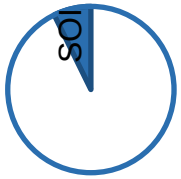
Automotive

- Transceiver CAN/LIN
- Brushless motor drive
- High T. gate drivers



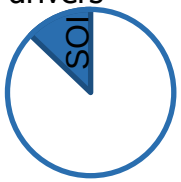
Communication

- AMOLED power supply
- AC/DC Power converter



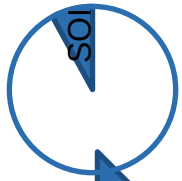
Consumer

- LED drivers
- 3-phase motor drivers (white good, air conditionner)
- Plasma display drivers



IT

- Desktop power supply
- Power over Ethernet



$CAGR_{2013\text{-}2016}$ power market = 7%

$CAGR_{2013\text{-}2016}$ power SOI smart cut™ = 20%

Conclusion

1. Power market is going smart
   - Power distribution is going Smart grid
   - Remote control of all power consumption for better global efficiency
2. Mix-voltage integration is key
   - Integrate different voltage requirements for remote control, logic, sensor, power conversion
   - Enable power efficiency (conversion and usage)
3. SOI provides better performances and smaller die
   - Simplify design cycle for time to market
   - High temperature and truly latch-up free operation
   - Thin SOI-BCDMOS design brings additional benefits (switching speed, low Rdson)
4. SOI for smart power is cost effective
   - Substrate performance impacts on chip design, size and cost
   - Optimized SOI design per application enable high competitive solution

Thank you for your attention