Mobile Phone RF Front End Integration Roadmap

March 17, 2015

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Agenda

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- Market Dynamics
- Smartphone Front End Block Diagram
- Block By Block Performance Analysis (SOC vs. SIP)
  - RF Switch
  - PA
  - Analog and Mixed Signal
  - MIPI: Gate Level
  - ESD
- Isolation Requirements
- Top Level Tools and Simulation Requirements
- Summary

Market Dynamics

Connect Everything

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Connected Devices Are Exploding

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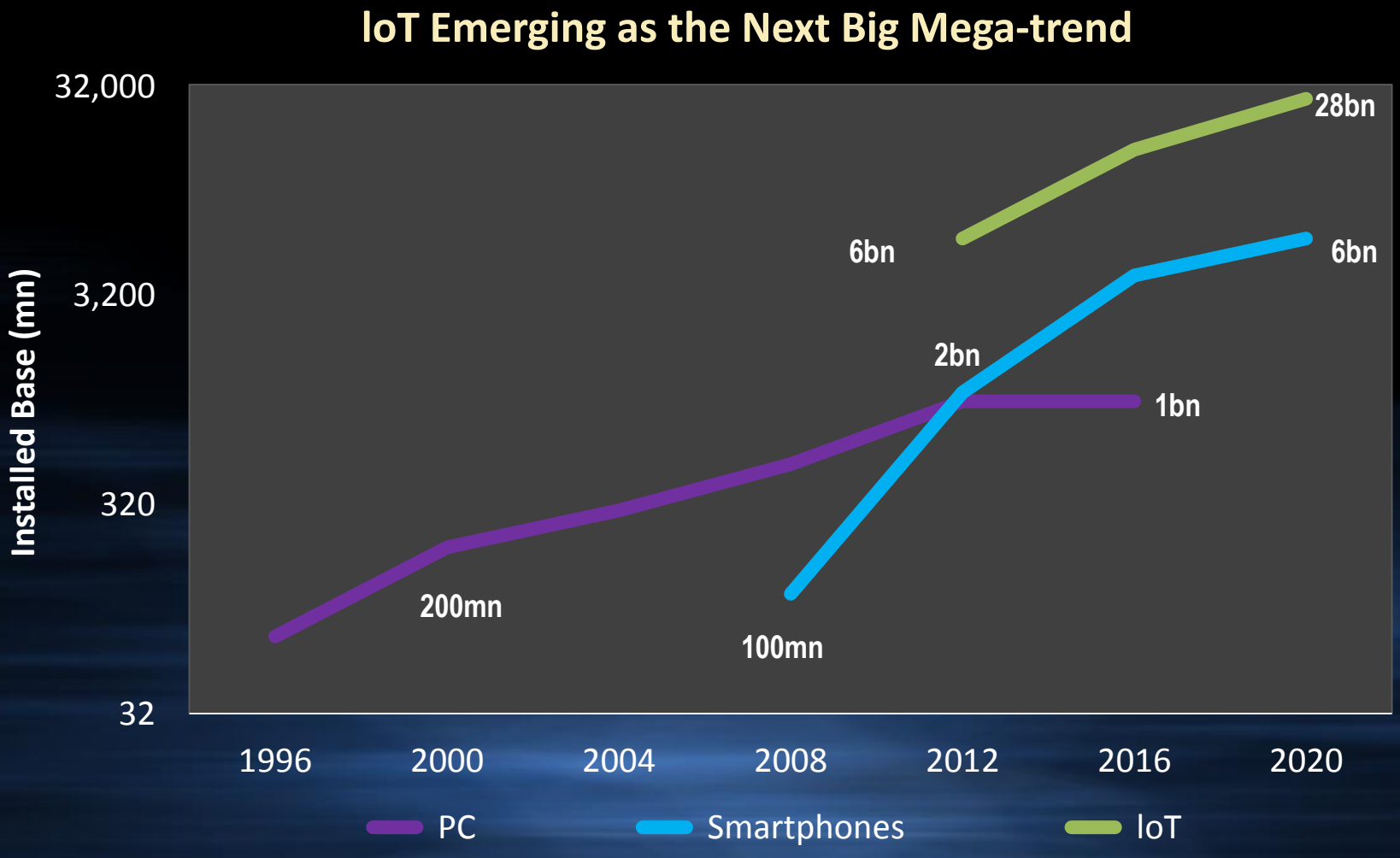

Y-axis is on a logarithmic scale

Source: IDC, Ericsson, Goldman Sachs Global Investment Research

Global Mobile Data is Exploding

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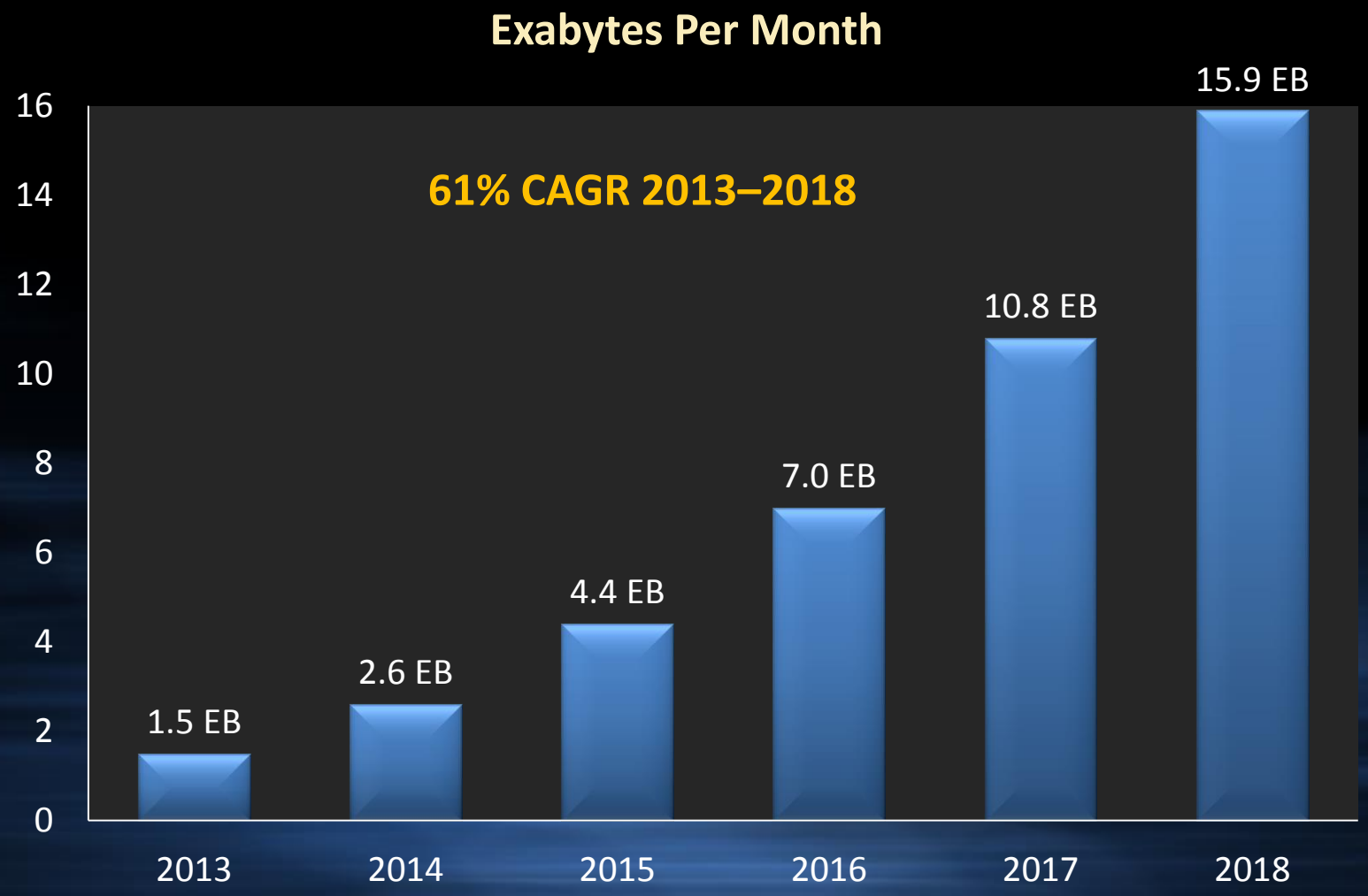

Source: Cisco VNI Mobile, 2014

Increasing Front End Requirements

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	2012	2014	2016E	2020E
LTE Rel	LTE Rel-11	LTE Rel-12	LTE Rel-X	5G
# CA Bands	2	3	3	5
MIMO	8x8	8x8	8x8	64X8
Proposed New Bands		5+	24	50
CA Band Combos	25	75+	172	300
Peak/Max DL	1.2Gbps	3Gbps	6Gbps	18Gbps

Increasing Front End Complexity

Expanding Band Count

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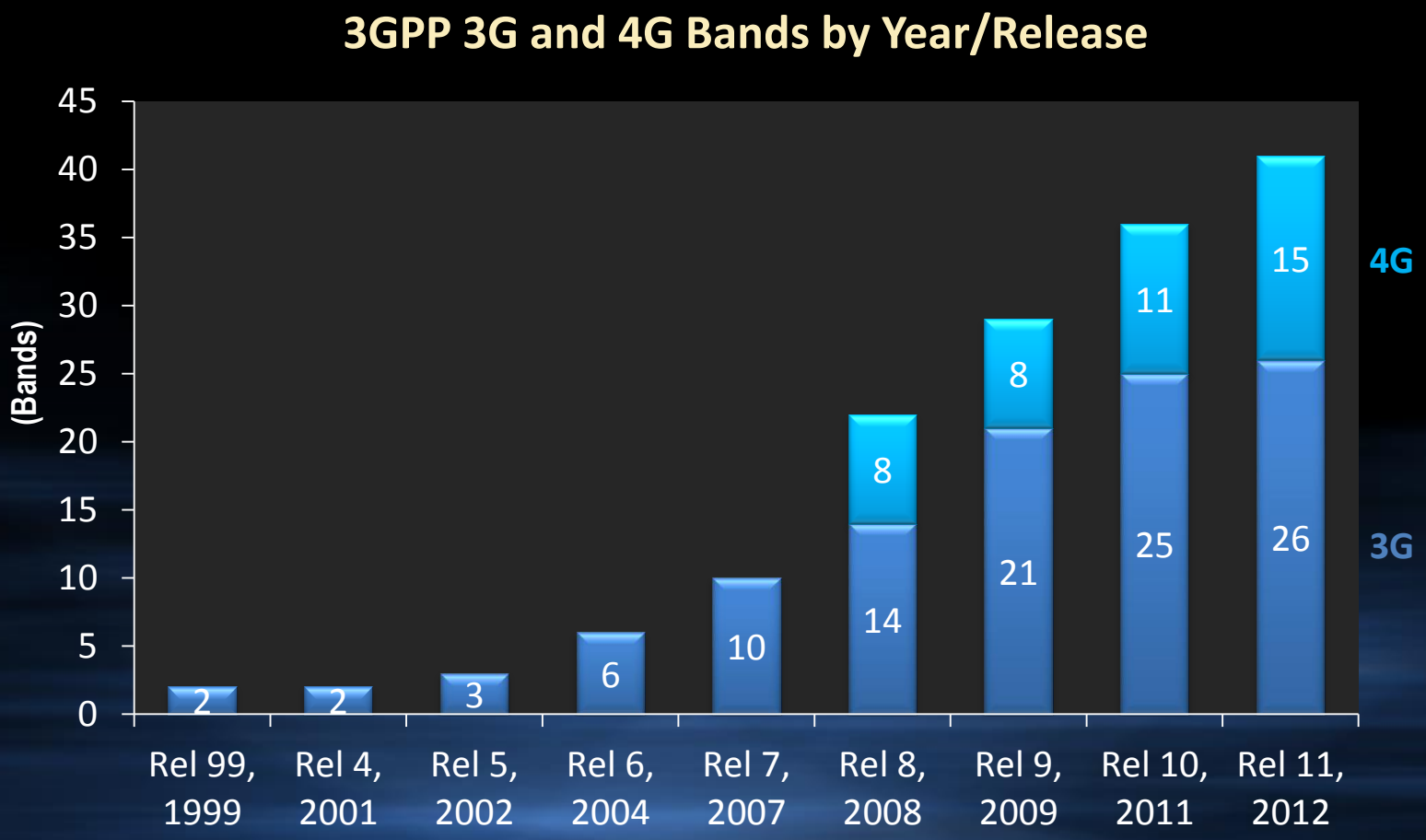

More Data = More Bands

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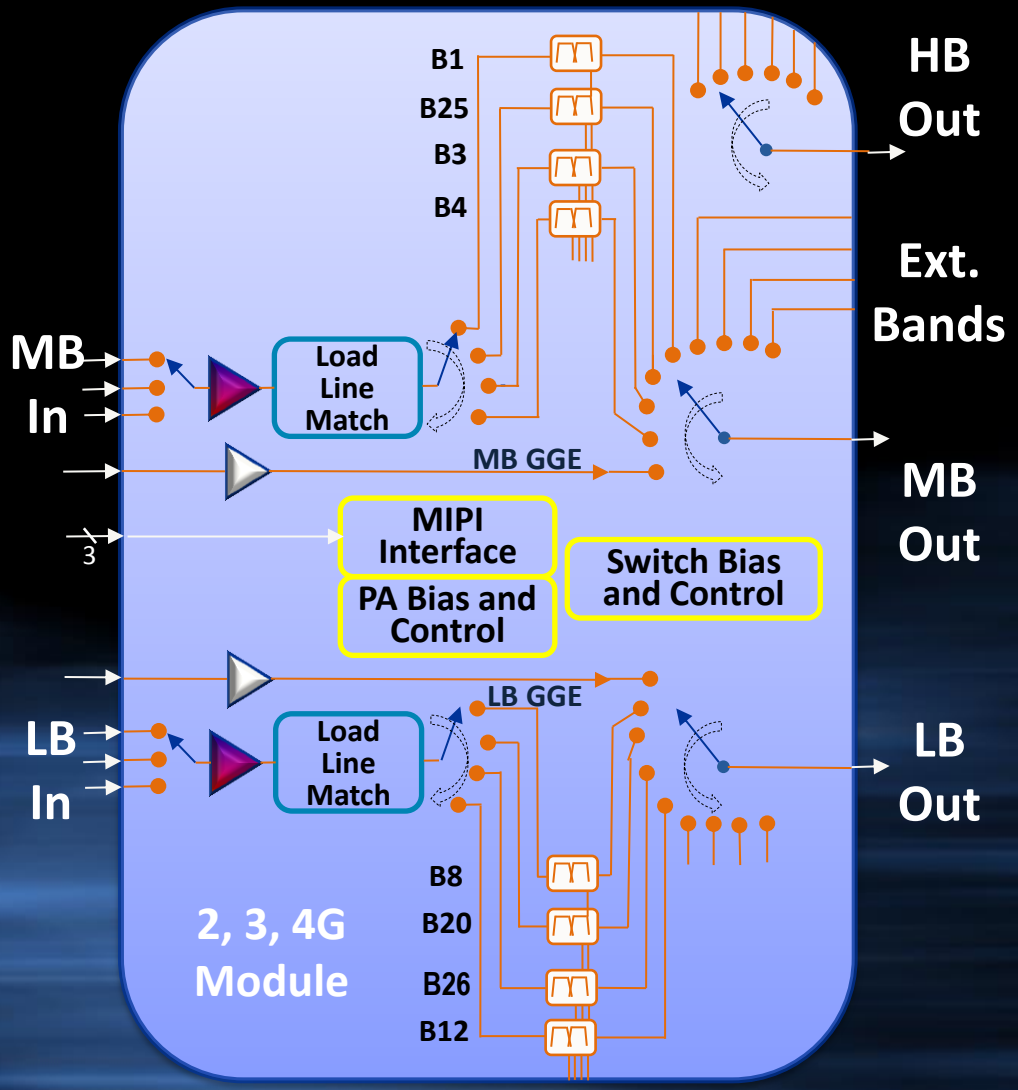
Cellular Smartphone Front End Block Diagram

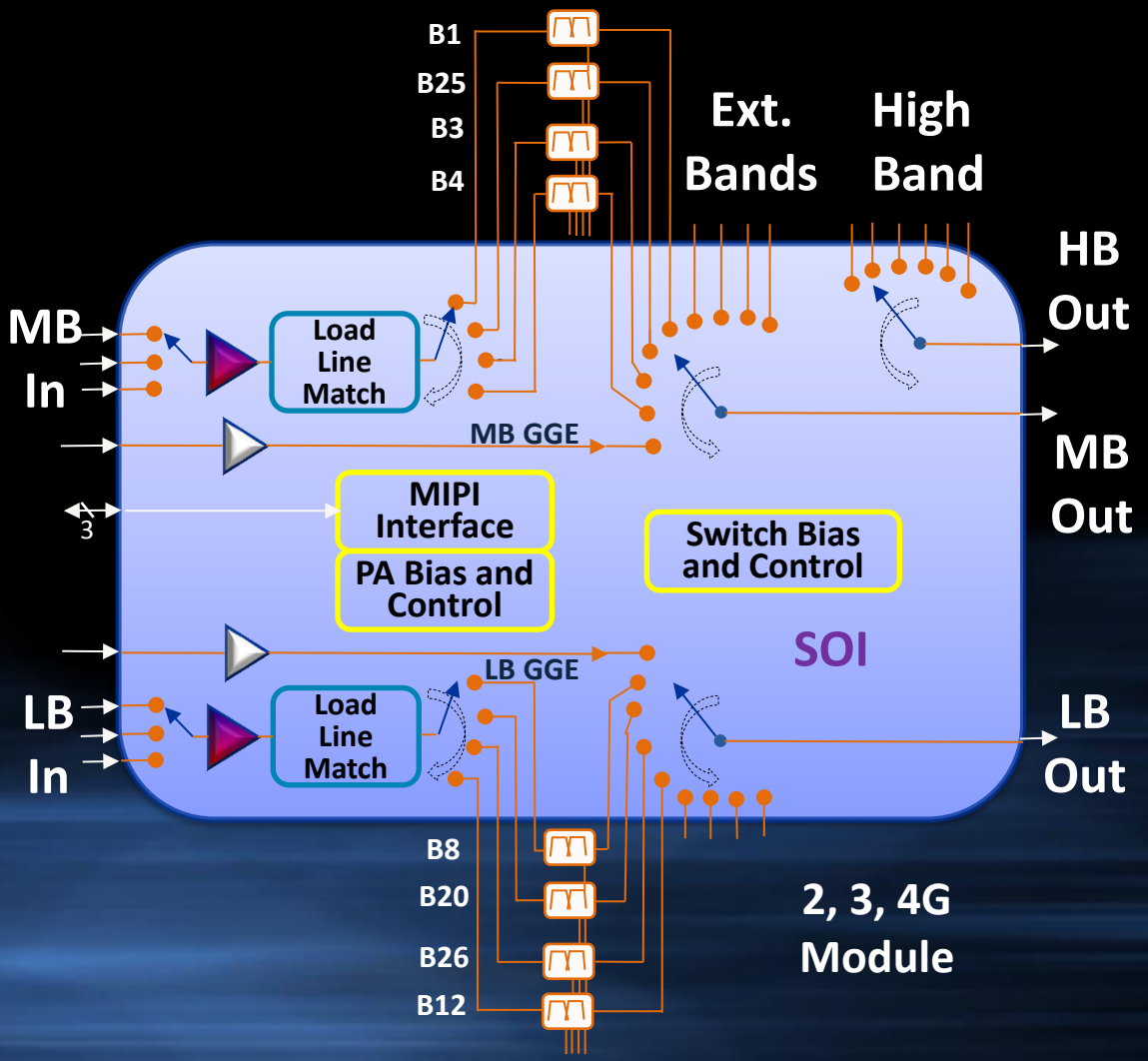
Mobile Handset Front End Block Diagram

- Smartphone
- 2, 3, and 4G
- 14 + Bands Typ.
  - LB 699 to 960 MHz
  - MB 1428 to 2170 MHz
  - HB 2300 to 2690 MHz
- Assumes High Band Module is Separate, but Could be Integrated



Mobile Handset FE Circuit Blocks

- RF Switch
- Switch Control
- PA
  - 4 to 6
  - Harmonic terminations
  - Load line match
- PA Control
- MIPI RFFE
  - 26 to 52 MHz SPI



Everything in Blue Could Be in SOI, But Should It Be?

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RF Switch

RF Switch Complexity in LTE World: Increasing Number of Bands

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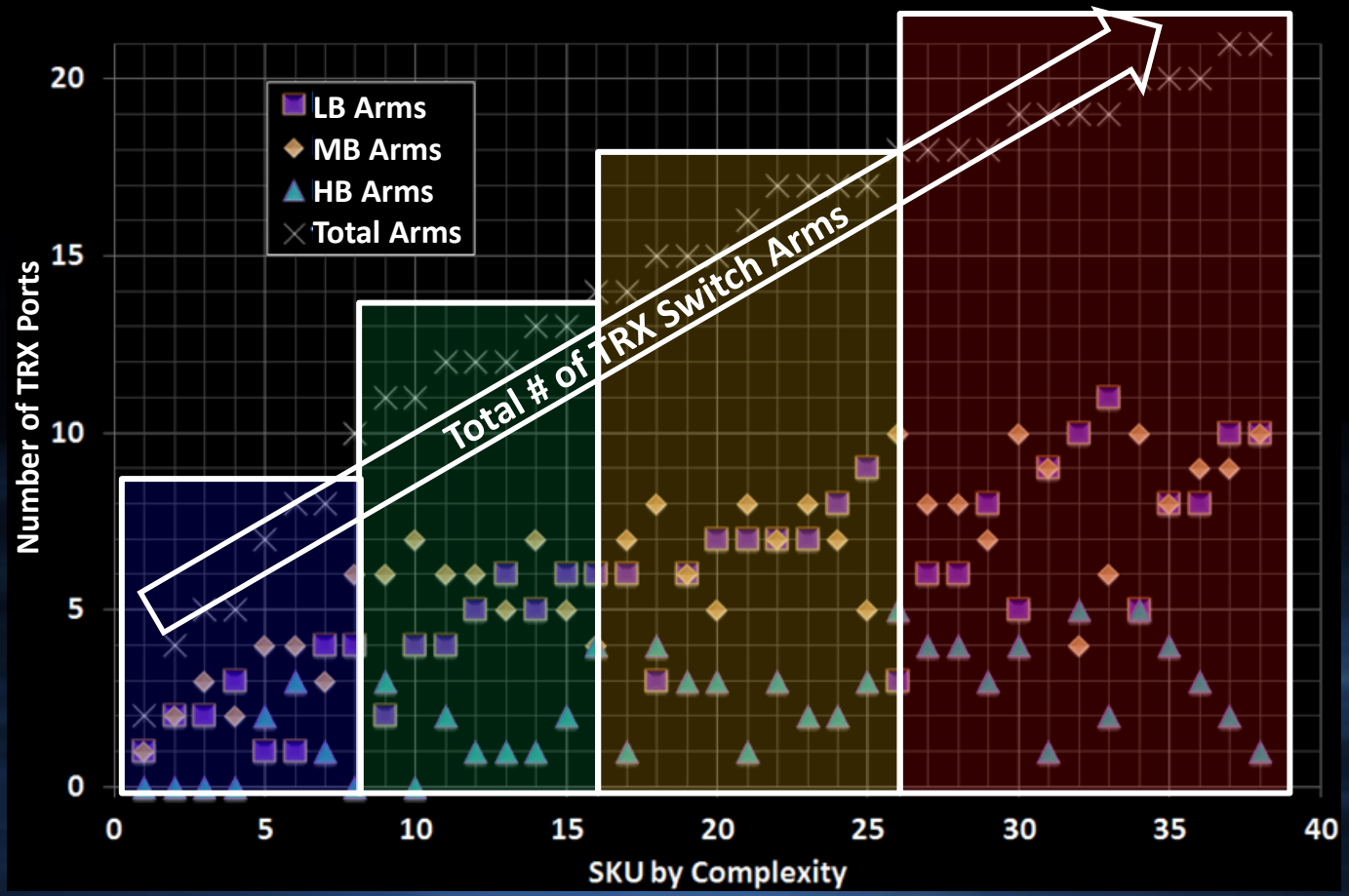

Total Switch Arms Required are Increasing

Inter-band Carrier Aggregation

Simultaneous Transmission of Multiple Bands

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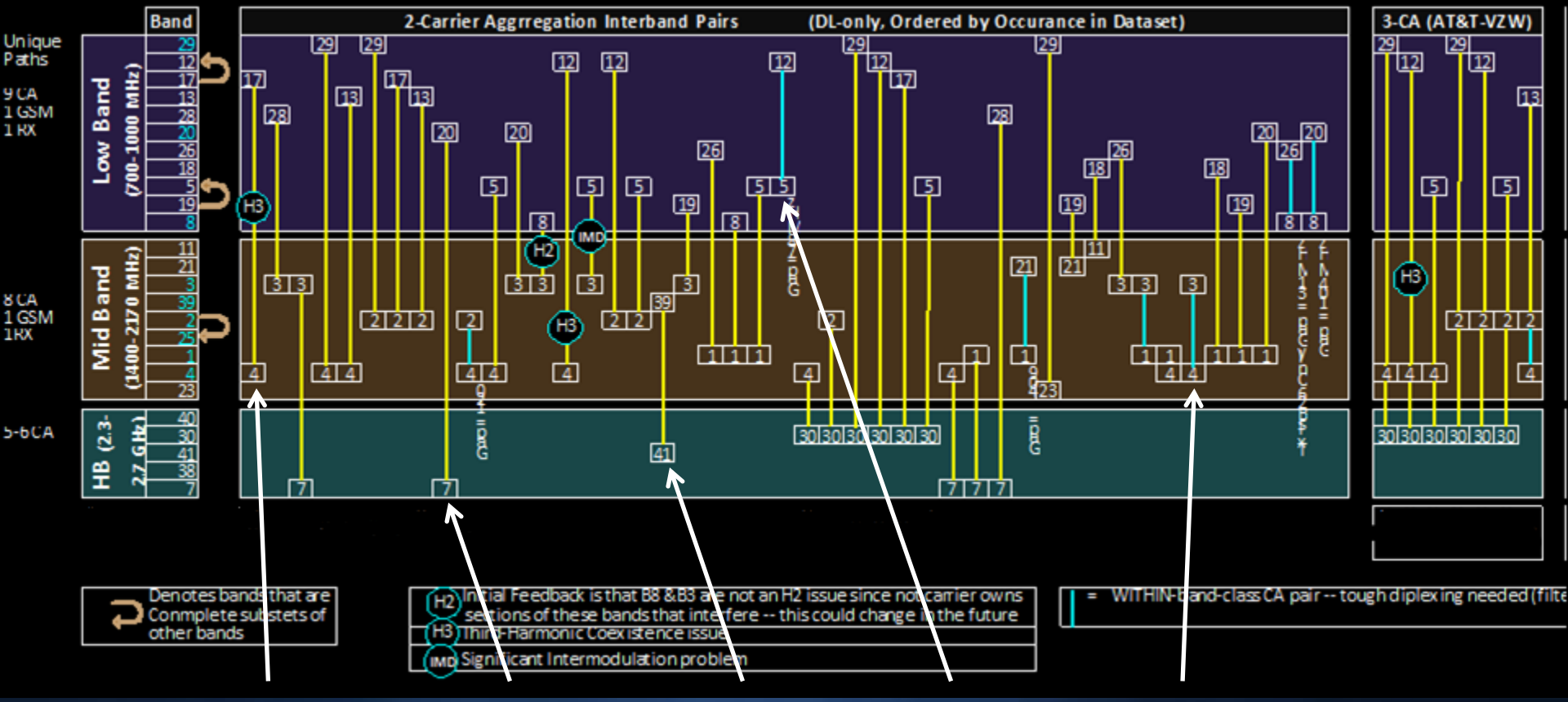
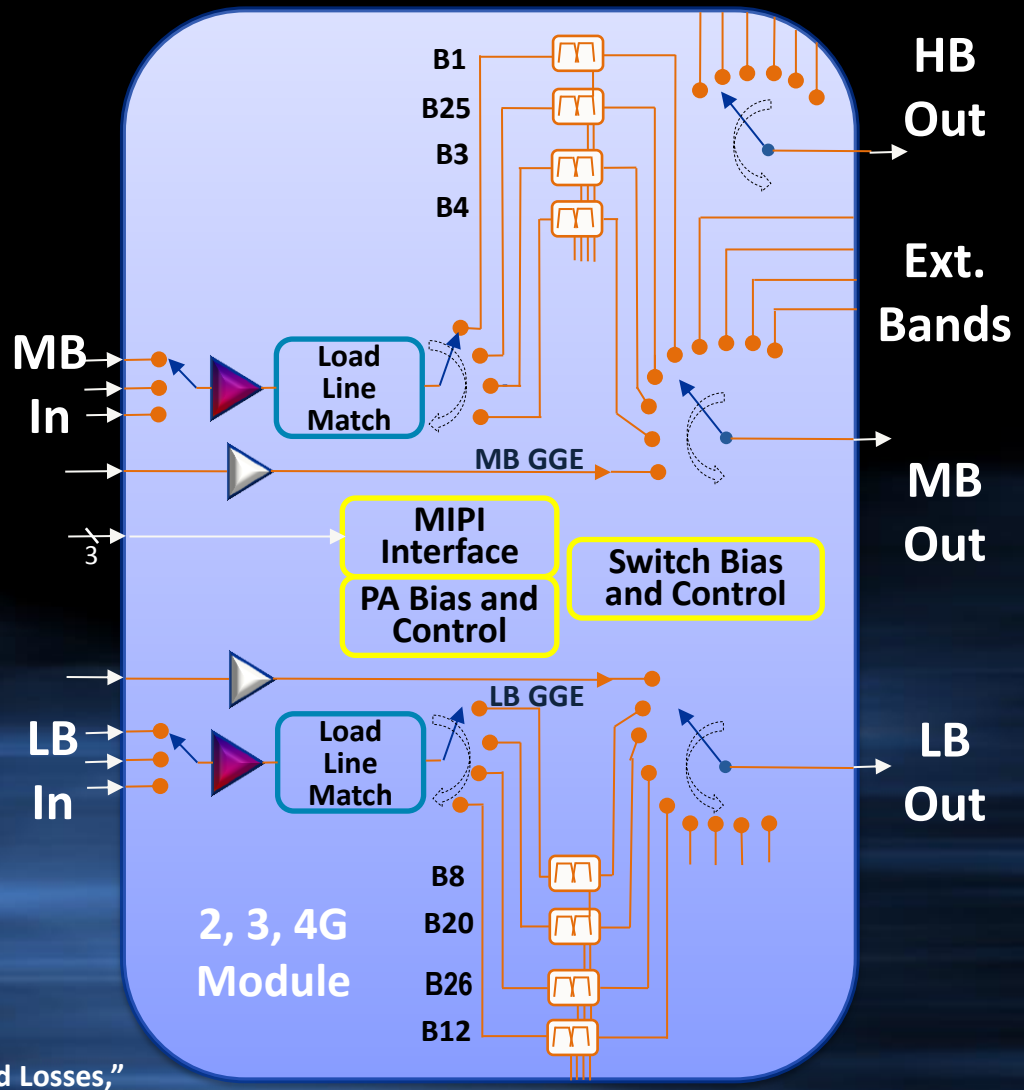


- Low/Mid, Low/High, Mid/High, Low/Low, Mid/Mid
- Low/Mid/High

RF Switch is Partitioned by Band to Allow for Diplexing of Bands

Front End Block Diagram

- CA the Three Bands
- LB
  - 699 to 960 MHz
- MB
  - 1428 to 2170 MHz
- HB
  - 2300 to 2690 MHz



J. Young "Carrier Aggregation, Quantifying Front End Losses," IWPC Chicago Meeting Sept. 16, 2014

Antenna Switch/Tuner Design

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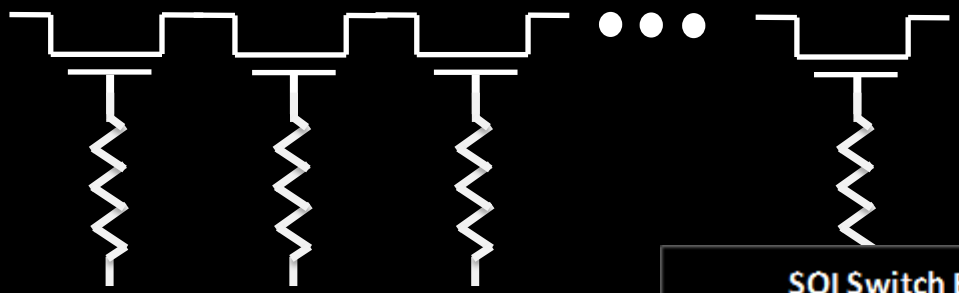

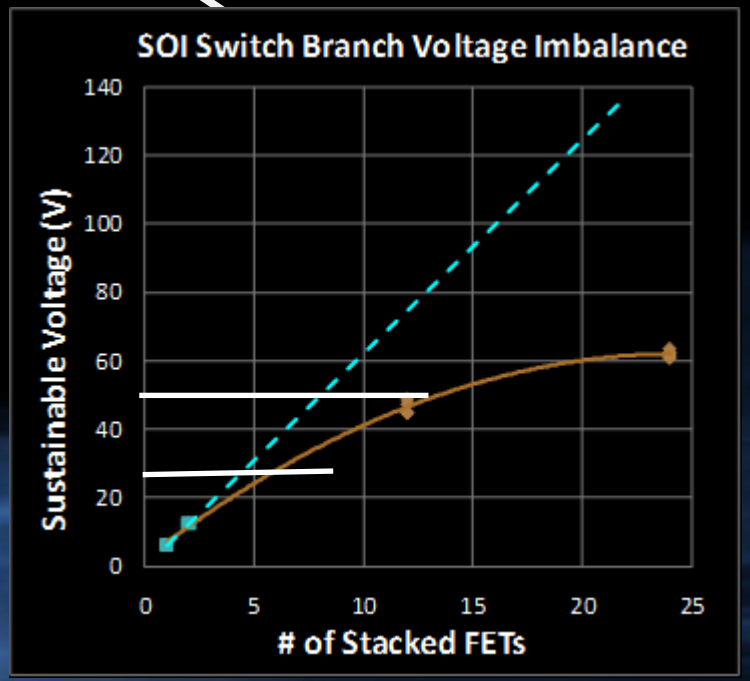

- Number of FETs in Stack
  - GSM Max. Pout and VSWR
    - ≈53Vp
  - 3/4G Max. Pout and VSWR
    - ≈25Vp
  - Each FET Can Sustain?
    - Technology dependent
    - Sub parasitics cause voltage imbalance

Peak RF Voltage Determines the FET Stack

Antenna Switch/Tuner Design

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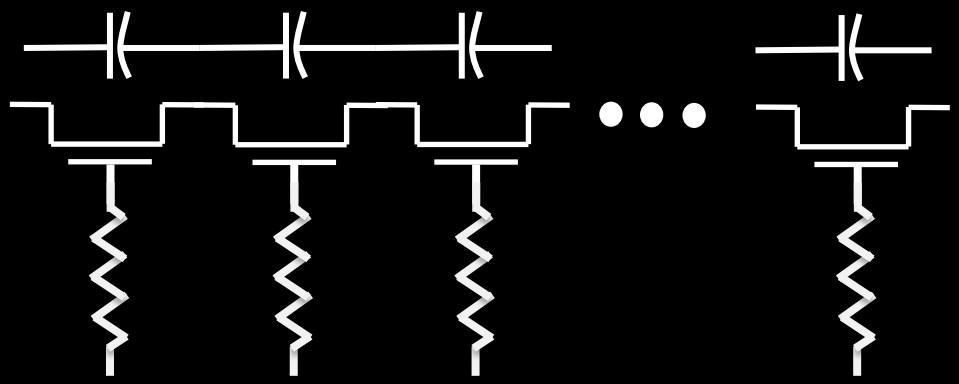

- Having established the number of FETS in the stack
- Minimize Coff to achieve specified off isolation
  - Use minimum L and scale W to specified Coff
  - Typically we will maintain around 30dB of isolation
- This determines Ron which is the dominate factor in insertion loss
  - Wα Ron

Optimize Coff

This Sets Insertion Loss

SOI Ron*Coff Process Improvement Lowers Insertion Loss

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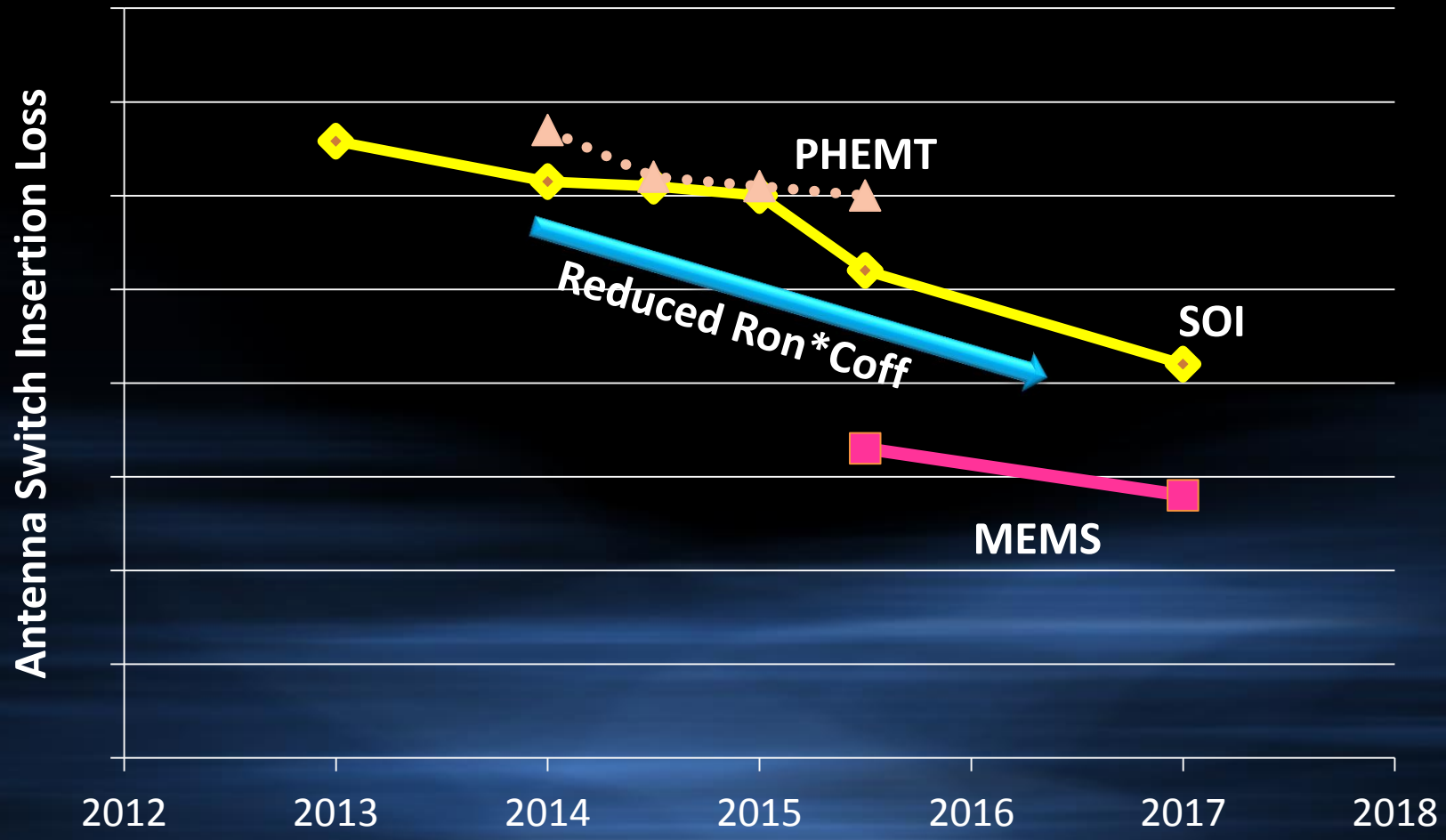
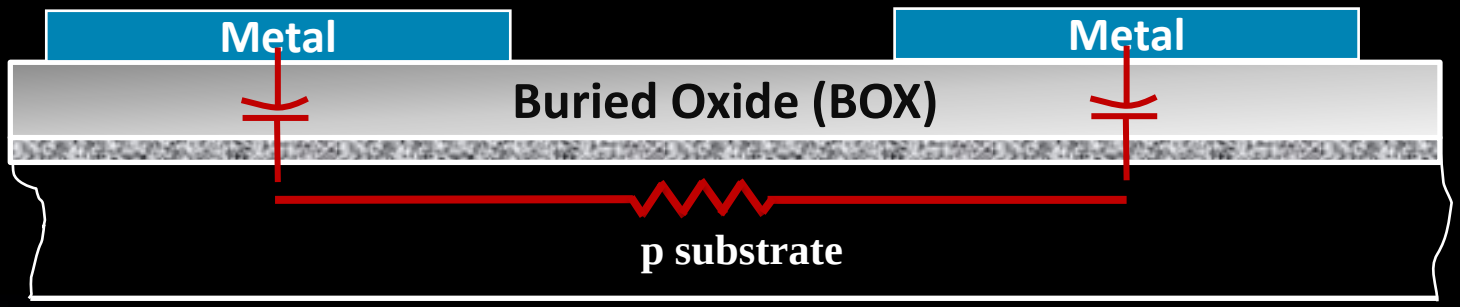
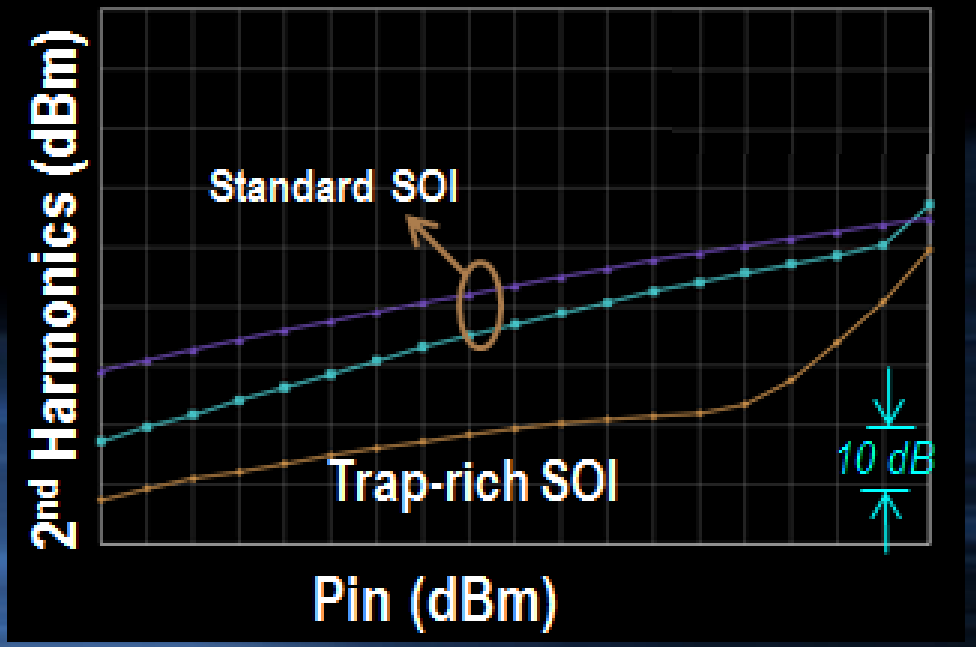


SOI Provides The Best Performance and Lowest Cost Solution

SOI Substrate: RF 2nd Harmonic



- Loss Decreases with Increasing Substrate Resistance
  - Typically use 1–10 kΩ/□
- Adding a Trap-rich Layer Reduces Loss and Improves Linearity



Managing and Reducing Substrate Parasitics Reduces Harmonics and IMD

RF Switch Summary

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	SOI	CMOS	pHEMT	MEMS
Insertion Loss	Acceptable	High	Acceptable	Best
Linearity	Acceptable	Acceptable?	Maybe Better	Best
Integration	Best	Best	Need an External CMOS Die	Requires MEMS on CMOS
Cost	Acceptable	Best	Higher	Very Expensive Today

SOI Provides The Best Cost and Performance Solution

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PA

PA Loadline Design

A Voltage Transformation

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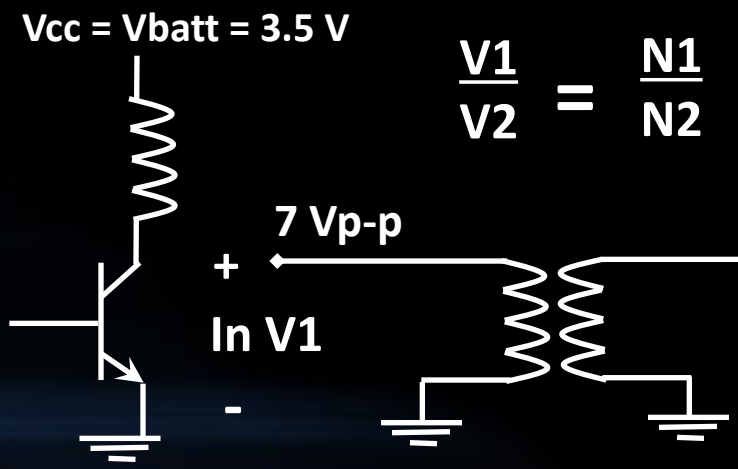
Converting the Battery Voltage to RF Output Power



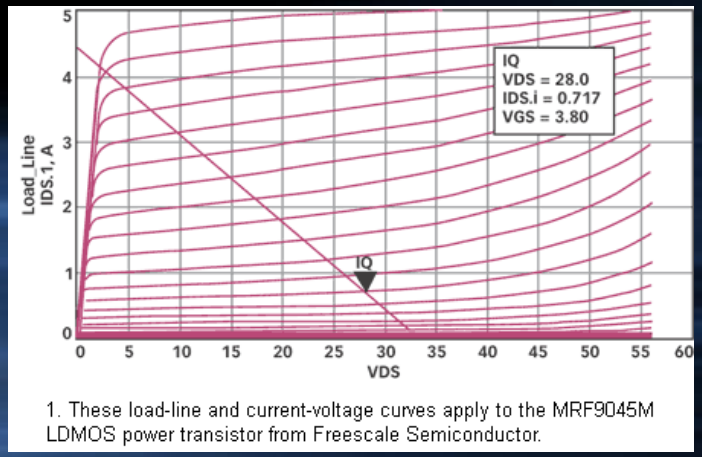
$$\frac{V1}{V2} = \frac{N1}{N2}$$

N1/N2 = transformer turns ratio
Pin = Pout (lossless transformer)

Pout = +34.6 dBm
50 Ohm
V2 = 33.6 Vp-p

$$P = \frac{V^2}{R} \qquad V_{rms} = Vp\text{-}p/(2*V2) \qquad Vp\text{-}p = 2Vcc$$

$$R = \frac{V^2}{P} \qquad R = \frac{Vcc^2}{2P_{out}} = \text{transistor load line}$$



1. These load-line and current-voltage curves apply to the MRF9045M LDMOS power transistor from Freescale Semiconductor.

Output Match Steps Up RF Voltage

SOI Transistor PA Scaling

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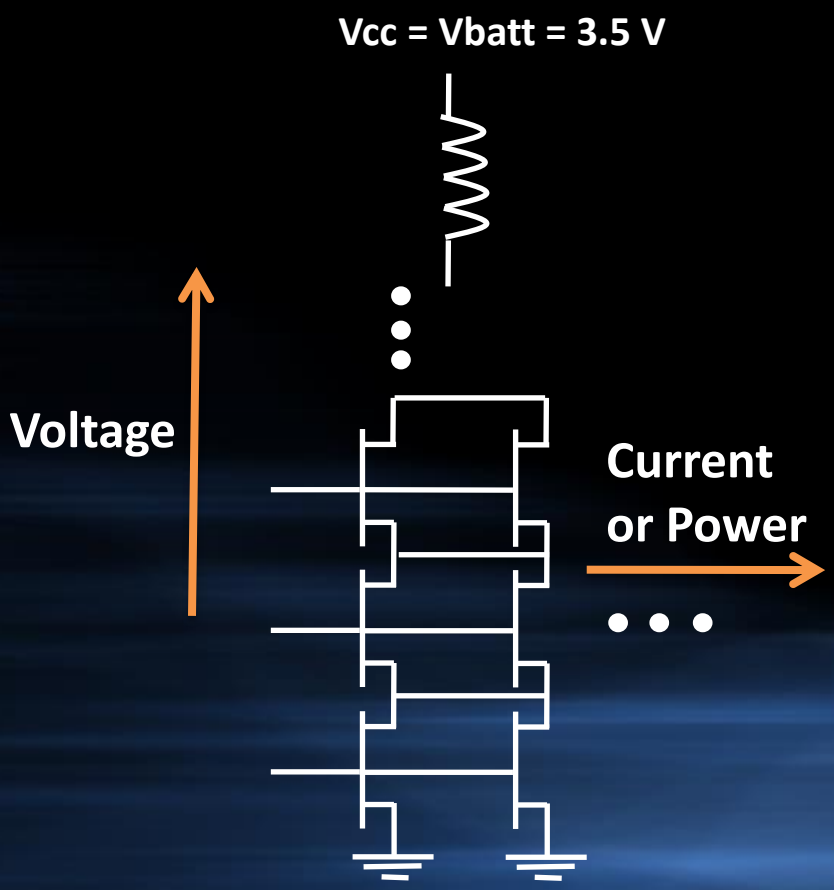

- Stacking Devices
  - Based on the device breakdown voltage
  - Shorter gate length: more devices
- Scale Width
  - To support peak current

Output Array Size Does Not Scale with Gate Length

PA Loadline Design

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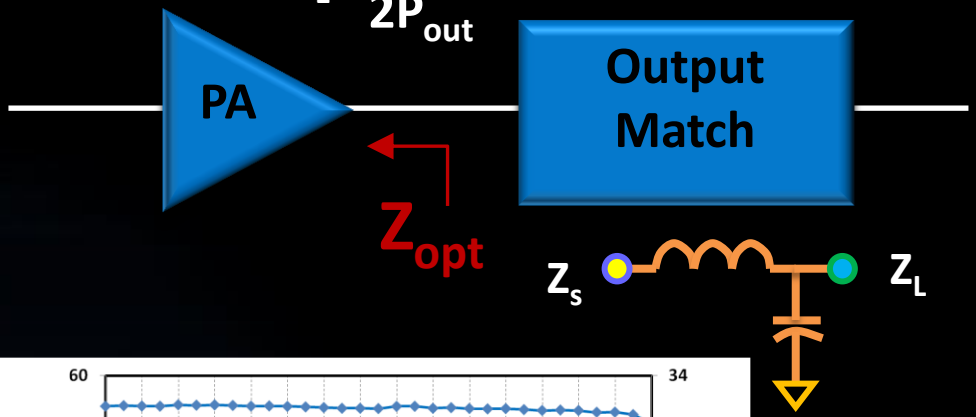
$R_L = \frac{Vcc^2}{2P_{out}}$ = transistor load line

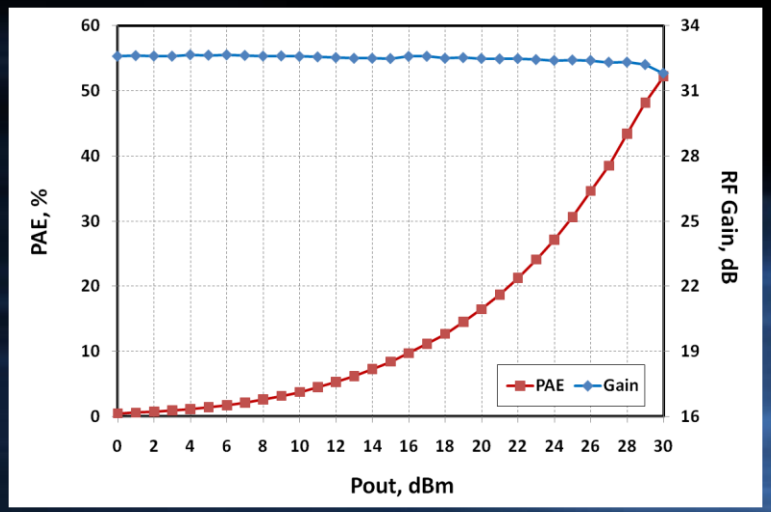
P_{out} is saturated output power

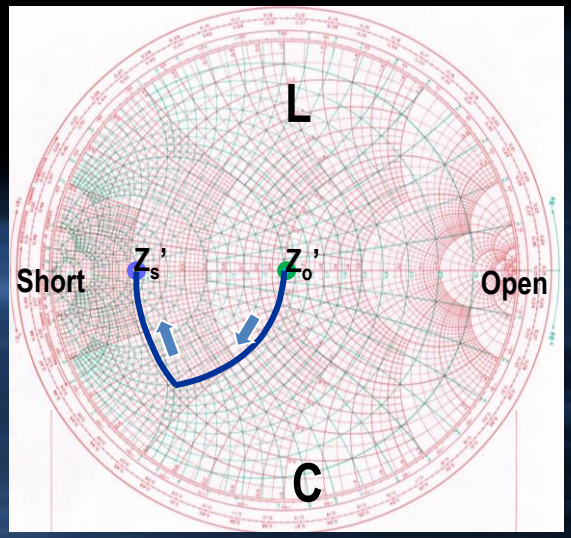
Vcc = 3.5 V battery

$P = V \cdot I$

$R = V / I$







Impedance Transformed with LPF

Metal Thickness vs. Inductor Q
2 GHz and 2–3 nH

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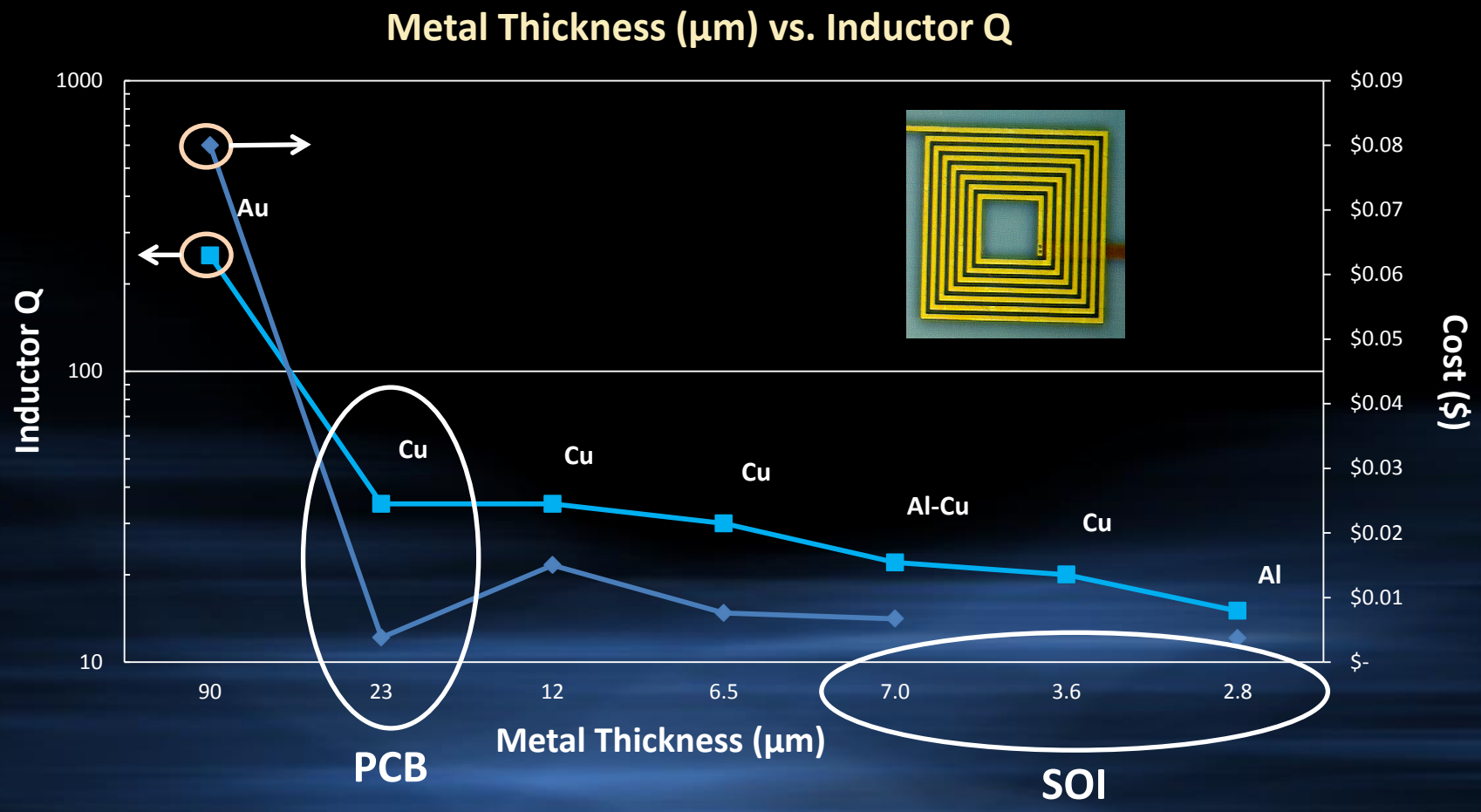
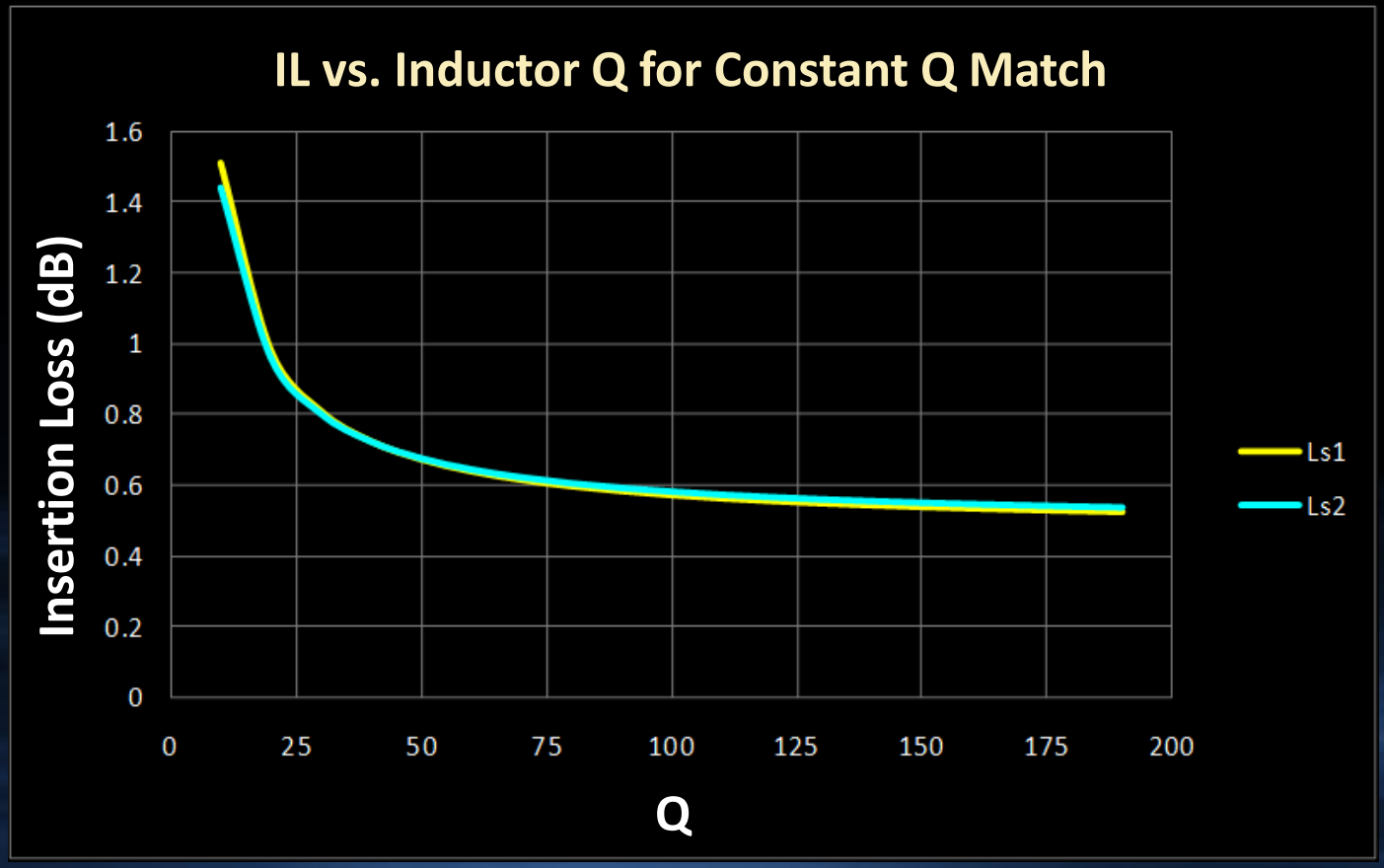


On Die SOI Match is Costly and Provides Low Performance Relative to PCB

Output Match Network (OMN) Loss vs. Inductor Q



- 865 MHz, 3 Ohm Load Line
- Capacitor ESR = 0.05 Ohms

Q of the Inductor Determines the Loss

SOI/CMOS vs. GaAs HBT PAE

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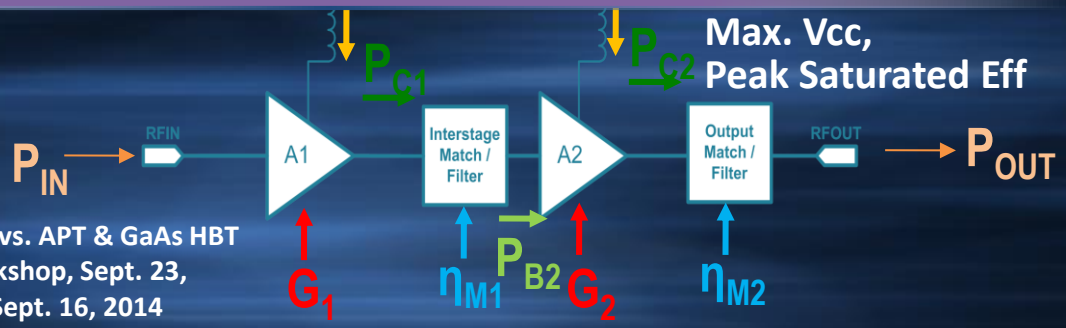
Technology	Drain or Col. Eff. η_{C2}	Output Match Loss η_{M2} (dB)	G_2	Inter-stage Loss η_{M2} (dB)	Driver Eff. η_{C1}	PA PAE Point A
GaAs HBT	89%	-0.65	14	-0.5	50%	71%
Measured HBT						66%
SOI	75%	-0.65	14	-0.5	40%	60%
Measured CMOS Amalfi[4]						50%
Reported CMOS Nujira [5]		57%	14	-0.5	40%	54%
SOI Carrara, Presti, et al. [6]	72%	-0.65	14	-0.5	40%	57%
CMOS 65nm [7]	70%	-0.65	14	-0.5	40%	56%
Peregrine SOI PA [9]	72%	-0.65	14	-0.5	40%	57%
SOI+on Die Match	75%	-0.8	14	-0.5	40%	58%



J. Young "Mobile Handset PA Performance. ET vs. APT & GaAs HBT vs. SOI/CMOS", 2014 International RF-SOI Workshop, Sept. 23, 2014, Shanghai, China; IWPC Chicago Meeting Sept. 16, 2014

SOI Device PA PAE Must Improve to Compete with GaAs HBT

PA Summary

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	SOI/CMOS	GaAs HBT
Pout	Acceptable	Acceptable
PAE	OK?	≈10% Better
Linearity	Challenging	Best
OMN Loss	Higher	External – Low Loss
Integration	Best	Requires External CMOS Controller
Die Size	3–5X	1X
PA Solution Cost	High	Low

GaAs HBT Provides the Lowest Cost with the Highest Performance

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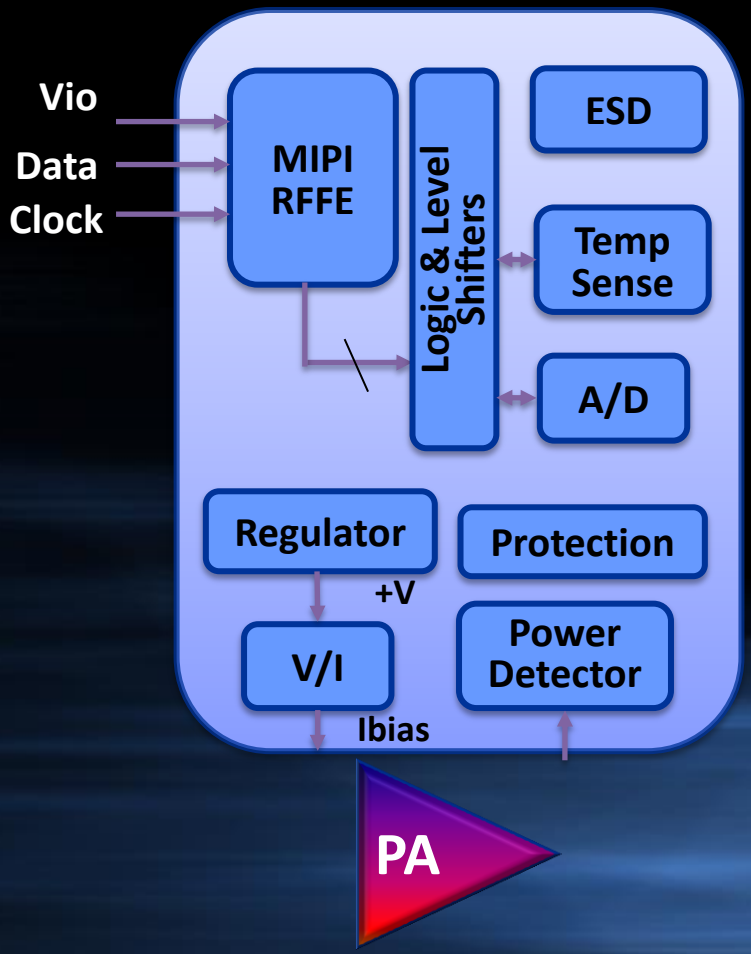
Mixed Signal

Digital and Analog Sections
PA Support



- Analog / Mixed Signal Section RF Switch Example
  - Band gap
  - Voltage regulator
  - A/D
  - V to I
  - Temp. sensor
  - Power detector
- MIPI
  - ≈ 5K gates
  - Needs a fine geometry to minimize size (<0.18 u)
- ESD Protection

Many Analog and Mixed Signal Circuits Required Place in a Low Cost CMOS Process

Digital and Analog Sections
RF Switch Support

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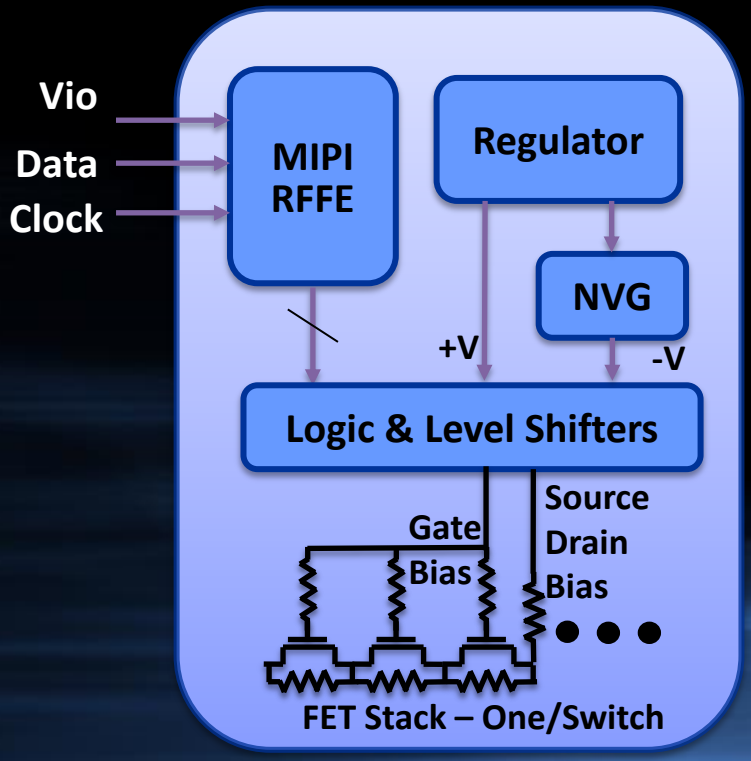


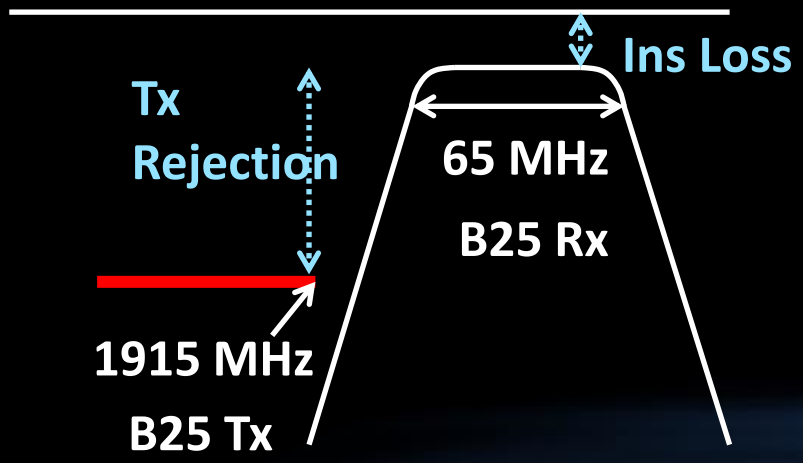
- Analog / Mixed Signal Section RF Switch Example
  - Oscillator
  - Band gap
  - Voltage regulator
  - Negative voltage generator

On the Die with the SOI Switch

Filters

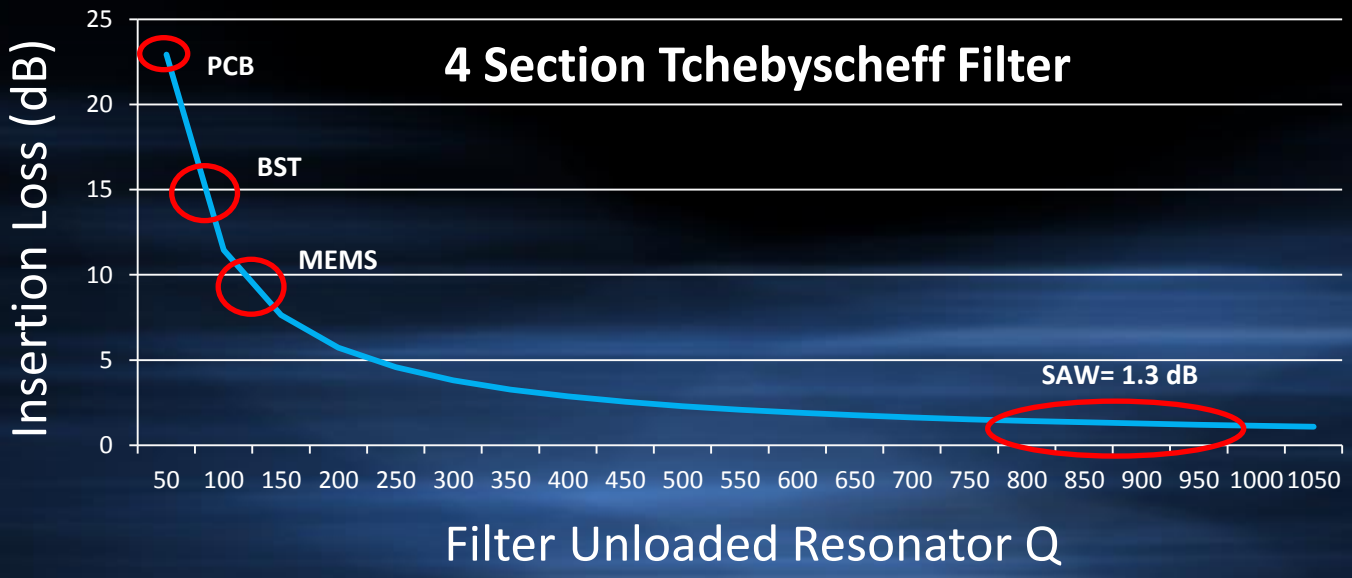
B25 RX Band Pass Filter Analysis

- Band 25
  - Passband RX 1930–1995 MHz
  - Rejection 1850–1915 MHz, >40 dB
- Calculation
  - W1=1930, W2=1995, Wt=1915
  - $W'/W_1' = (2/\omega)((Wt - W0)/W0) = 1.45$
  - Where $\omega = 2(W2-W1)/(W2+W1) = 3.3\%$
  - And $W0 = (2*W2*W1)/(W2+W1) = 1961.96$
- Filter
  - 8 section 0.2 dB Tchebyscheff (0.5 dB Ripple 7 Section Filter)
    - Tx rejection = 44 dB



Conclusion

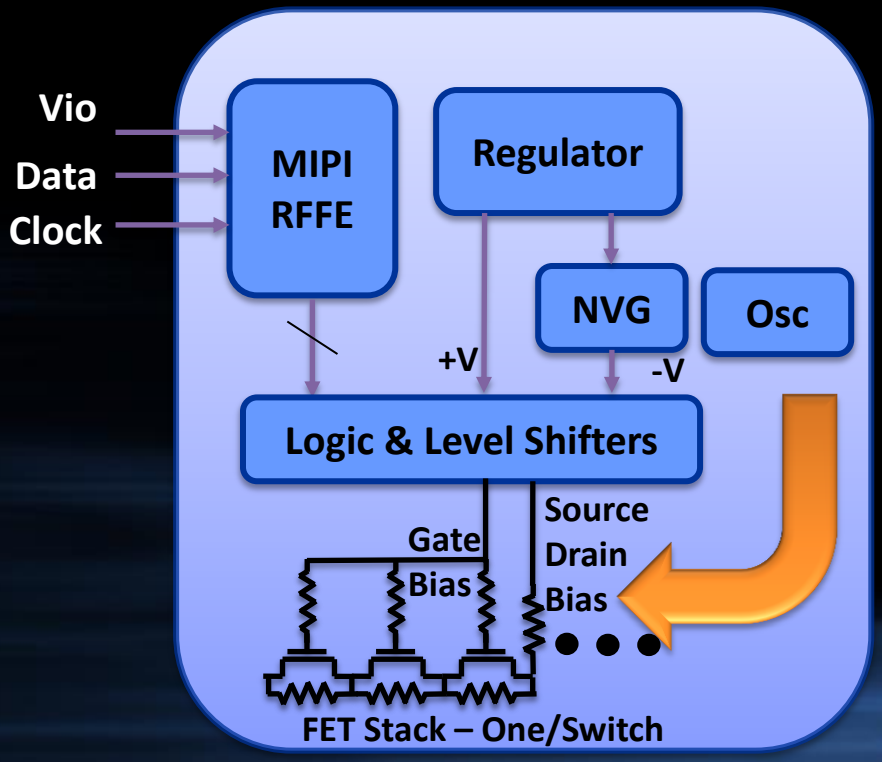
- Using a MEMS Capacitor and Inductor Tunable Filter
  - Unloaded combined Q of 100
- SAW Filters Provide the Q Necessary for a Low Insertion Loss



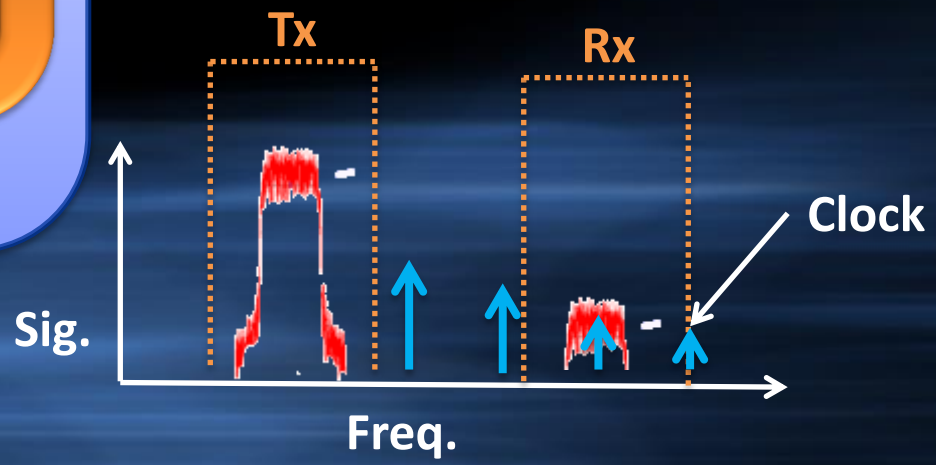
SAW or FBAR Filters are Required Today

Isolation

Clock Isolation



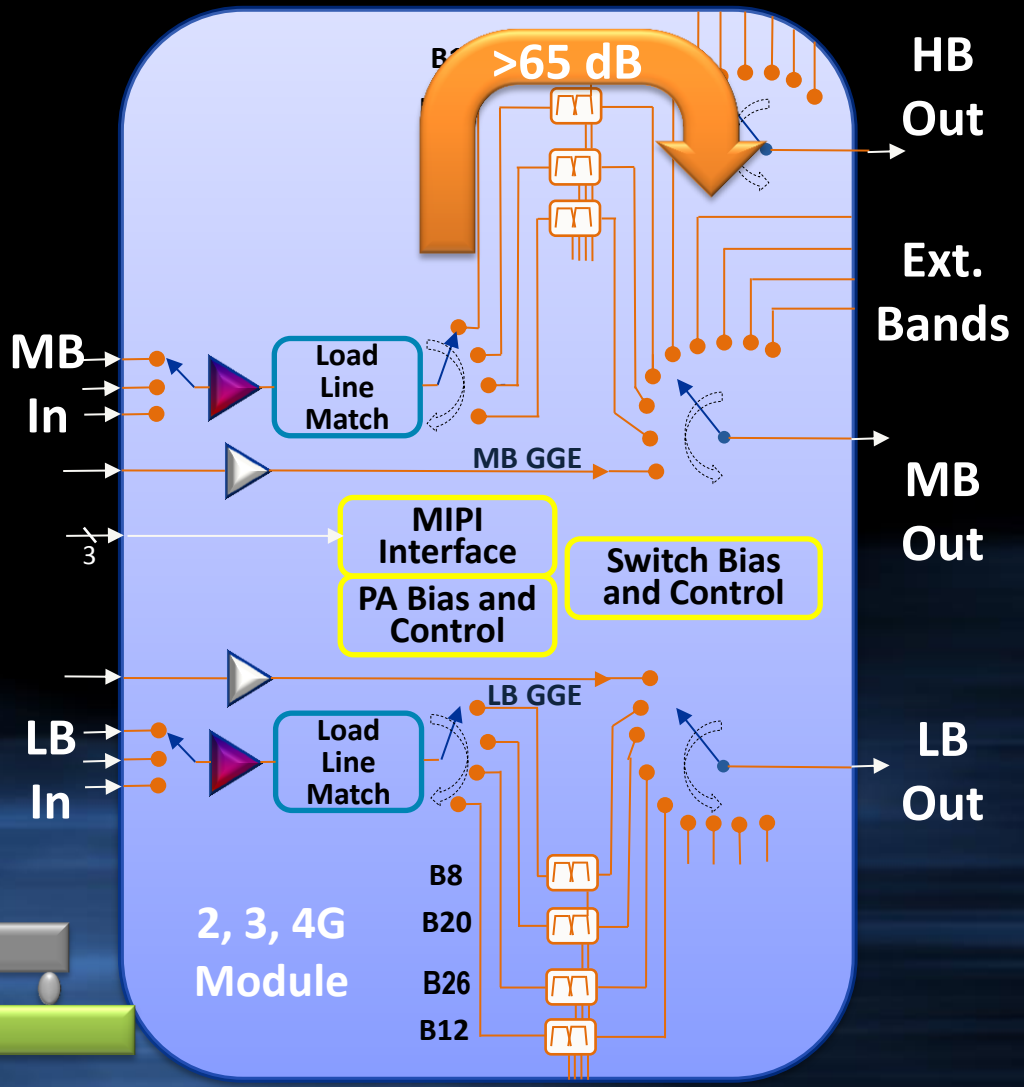
- Clock / Oscillator Noise
  - Can be conducted or radiated noise
  - Intermodulated clock noise onto the RF signal must be <110 dBm within the Rx passband



Clock Must Not be Present in the RF Switch

Tx to Antenna Isolation

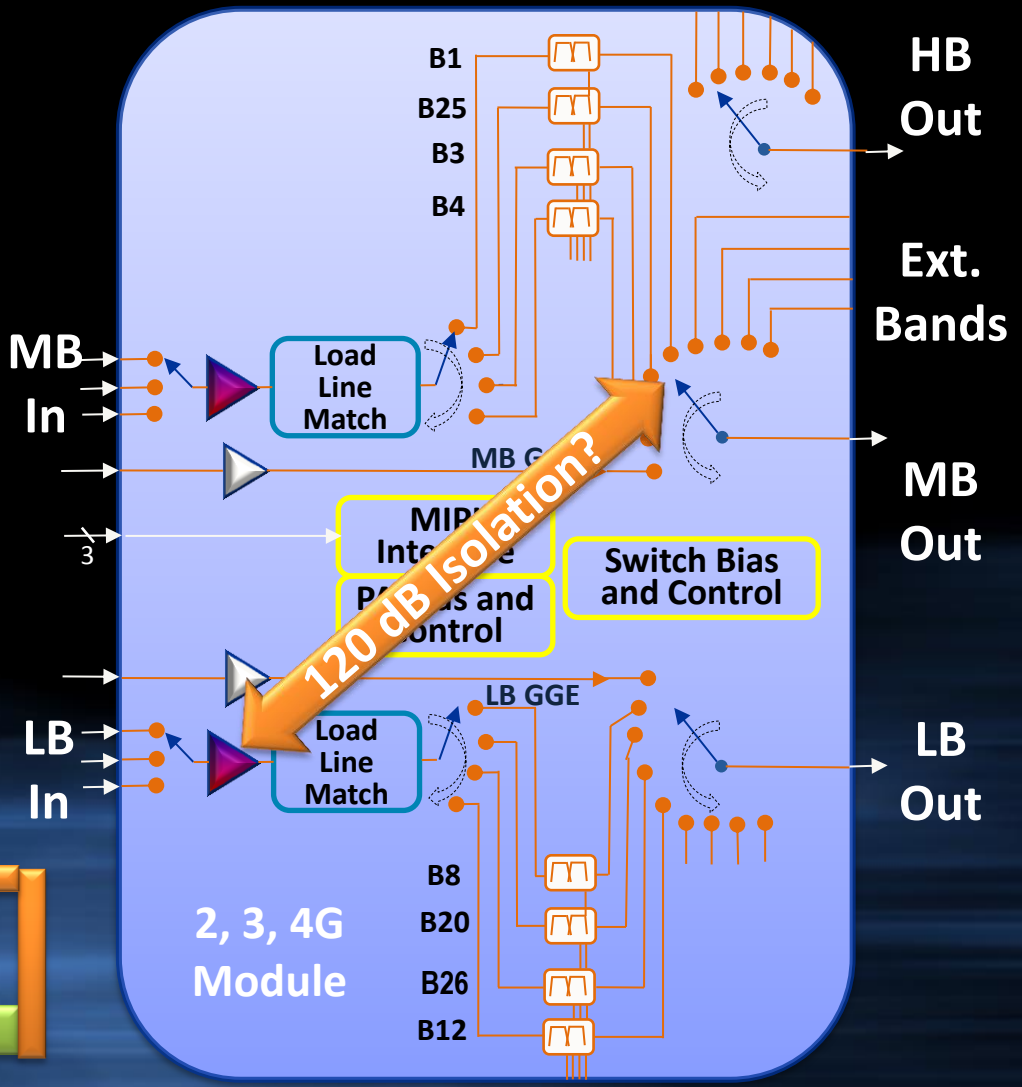
- Duplexer Tx to Ant Typically has >55 dB of Isolation
- SOI IC Should Have >65 dB of Isolation
- Typically Only Accomplished with a Flipped Chip Package and Careful Design of Routing
- This is Only One of Many RF Isolation Requirements in the Design



TX to Antenna Isolation Must be >65 dB to Avoid Desense

Tx to Antenna Isolation

- PA B12 3Fo is B4 Rx Band
- Need >120 dB of Isolation
- SOI SOC?
- Integrated Shielding in the Package



PA to Antenna Isolation Must be >120 dB to Avoid Desense

Design, Simulation and Test with High Integration

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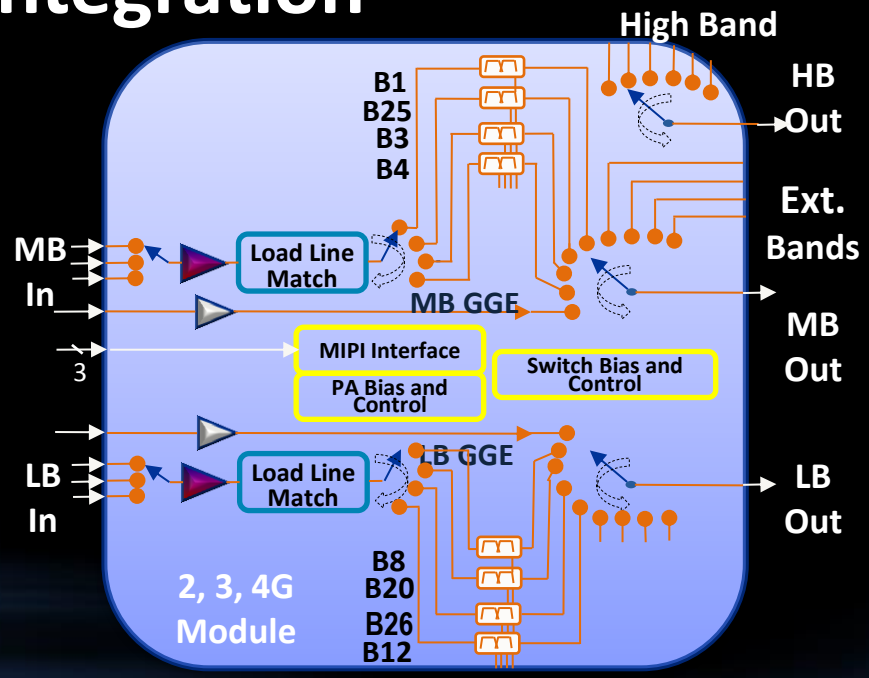

SOI Process

Ron*Coff
Thick Metal
Linear Substrate
High Isolation

Interconnect

Flip Chip
On Substrate
Integrated Shield
Transmission Lines

Functions

PA
RF Switch
Power Control and MIPI
Analog/Mixed Signal
Filters
ESD Protection

Sim. and Des. Tools

Harmonic Balance
Transient
2D/3D EM
RTL Compiler
NCSIM (Digital Sim.)

Layout

DRC, LVS, Antenna
Auto Router, Digital and Analog

Full Functional RF Test

Automated
Automated Data Analysis

Extremely Difficult and Time Consuming to Design, Test, and Analyze

Customer's Expectation

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1. First Skyworks Engagement
2. First Samples in ~6 Months
3. Total Functional Maturity in First Sample
4. Spec Compliant in 10 Months (or Less)
5. Production Ramp in 12–14 Months (or Less)

Design Efficiency Must Be High: Design, Simulate, Fab, and Test
SIP Provides the Fastest Time to Market

RF SOI, RF CMOS, and BiCMOS
Skyworks Shipments

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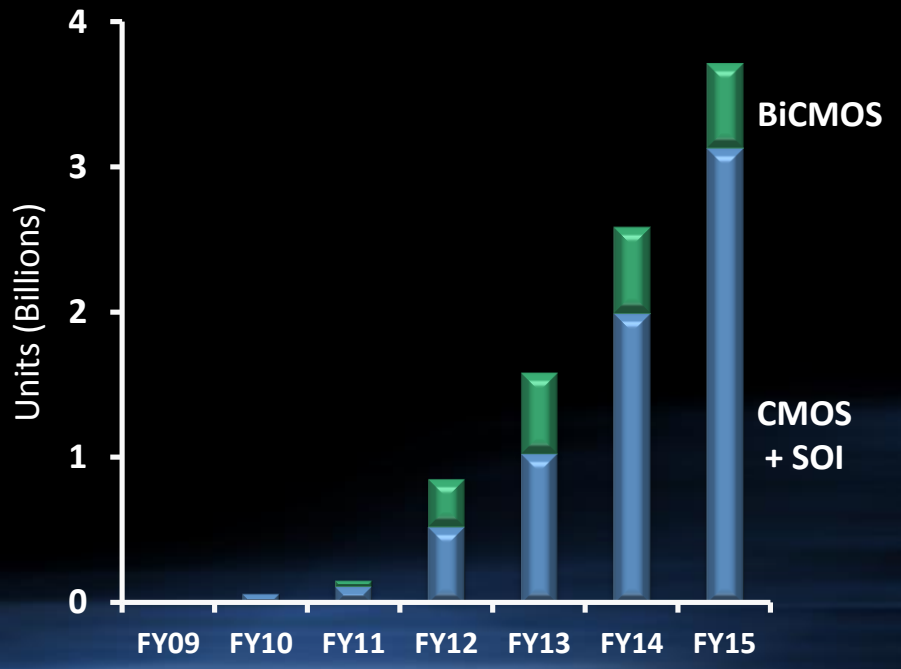
- Shipped > 6.5B RF SOI Devices
- Shipped > 2B Silicon BiCMOS PAs (Wi-Fi)
- Shipped > 150M CMOS Cellular PAs
- Experienced RF CMOS or SOI Leader
- Long History of Development Activity



SOI is Clearly a Big Part of the Growing Mobile Market

Summary – The Best Solution

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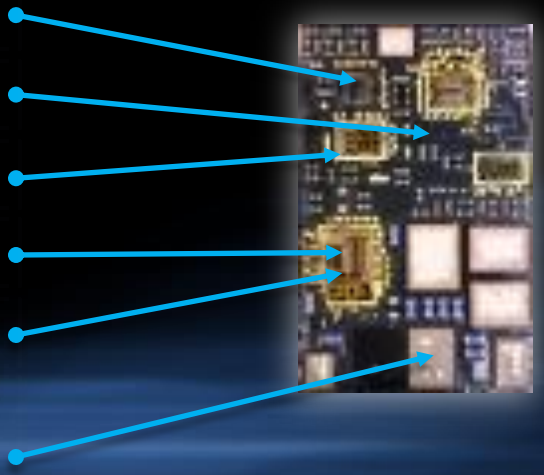
Block	Technology of Choice	Primary Reason
PA	GaAs HBT	PAE and Cost
PA OMN	PCB	Low Loss/ High Q
PA Controller	CMOS	Cost
RF Switch	SOI	Cost/Performance
Switch Controller	CMOS/SOI	Cost
MIPI RFFE	CMOS	Cost
Filters	SAW/FBAR	High Q



SIP Wins Based on Cost, Performance and Time to Market

References

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- [2] F. Raab, “Maximum Efficiency and Output of Class-F Power Amplifiers,” IEEE Transactions on Microwave Theory and Techniques, Vol. 49, NO. 6, June 2001.
- [3] J. Young, N. Cheng, “Multimode Multiband Power Amplifier Optimization For Mobile Applications” IEEE VLSI_TSA Conference, April 23 2013
- [4] Hee-Soo Lee, Andy Howard, “RF Power Amplifier Design Series Part 4: RF Module Design using Amalfi CMOS PA” 2012 Agilent Technologies, Inc., Webcast
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