RF Performance of Passive Components on State-of-Art Trap Rich Silicon-on-Insulator Substrates

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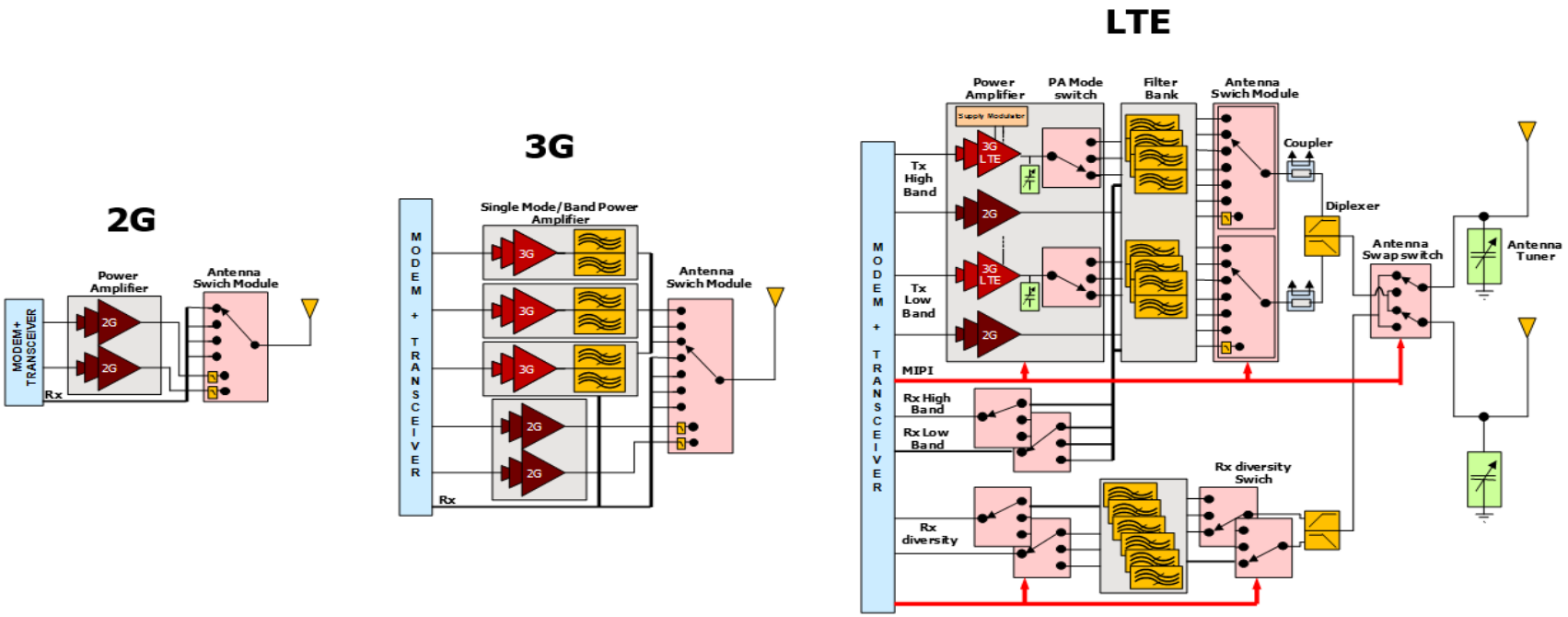
Outline

- Introduction on RF SOI Technology
- Soitec-SITRI Joint Development Program on RF SOI Technology
- CPW lines integrated on the HR-SOI and RFeSI substrates
  - Small signal characteristics: attenuation characteristic, and temperature effect on it
  - Large signal characteristics: the 2nd and 3rd harmonic, and temperature effect on them
- Spiral inductors integrated on the HR-SOI and RFeSI substrates.
- Conclusion

RF Front End Evolution (from 2G to 4G)

--access to what you want, when you want and where you want



Courtesy of Soitec

- More antennas → MIMO
- More frequency bands → high performance high-throw switches
  - → more low-throw switches
  - → more PAs, more filters
- Package (SIP) and module integration

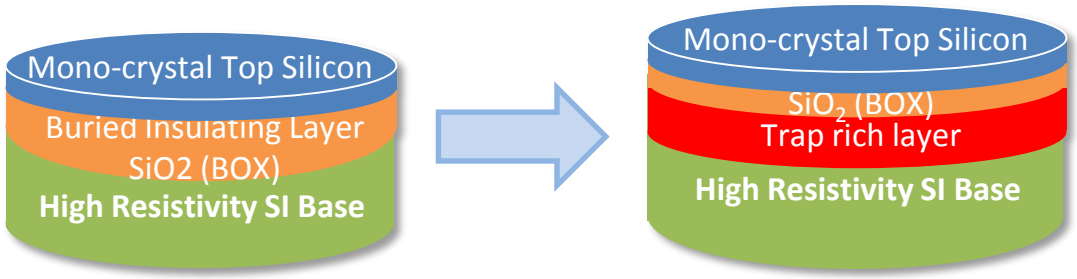
Soitec RFeSI Products
Enabling Performance to The RF Function

Cellular roadmap always requires more linearity

Network	Linearity (IIP3 in dBm)
2G	55
3G	65
4G LTE	72
4G LTE + CA	Up to 90

Source: Intel Mobile, L. Schumacher, Nov. 2012

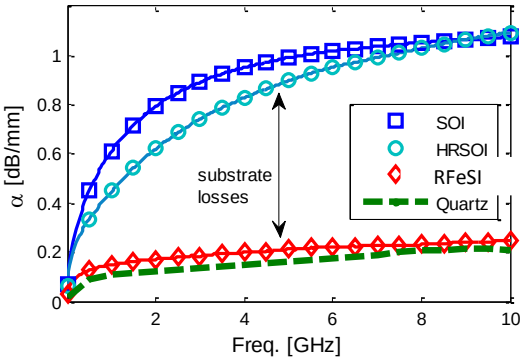
A trap rich layer is added to the standard



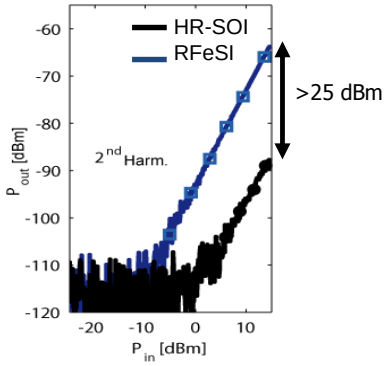
HR-SOI substrate

RFeSI SOI substrate

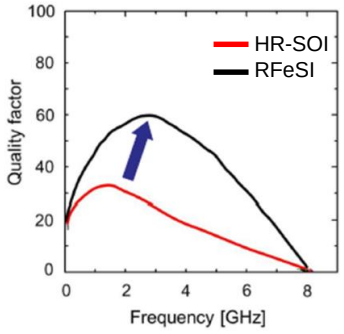
- Improve all RF critical parameters



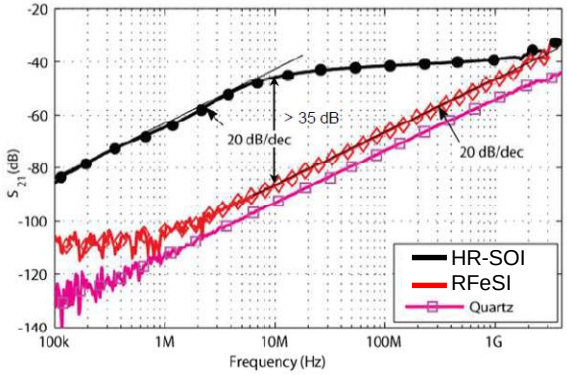
Insertion Loss



Linearity



High Q passives



Crosstalk

Source: UCL

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Soitec and Shanghai Industrial µTechnology research institute (SITRI) announce collaboration on high-performance RF-SOI technology

Aim is to develop next-generation SOI communication solutions focusing on the fast-developing Chinese RF ecosystem

Bernin (Grenoble), France and Shanghai, China, June 9th, 2015— Soitec (Euronext), a world leader in generating and manufacturing revolutionary semiconductor materials for the electronics and energy industries, and Shanghai Industrial µTechnology Research Institute (SITRI), a leader in "More than Moore" technology R&D and commercialization, announced today the signature of a collaboration agreement. The strategic partnership will enable both Soitec and SITRI to strengthen their leadership in high-growth wireless communications and the global market for radio-frequency (RF) applications, with a special emphasis on the fast-developing Chinese RF ecosystem.

The joint collaboration announced today focuses on developing RF-SOI (Silicon On Insulator) technology using advanced circuit designs based on Soitec's substrate materials and technologies.

"Experience shows that Soitec's engineered substrates can optimize RF-SOI technology and applications in terms of both cost competitiveness and power efficiency. This strategic partnership will enable us to push the limits of RF circuits and meet future connectivity needs," said Carlos Mazure, chief technical officer of Soitec.

"Enhancing RF signal integrity is a key focus of the mobile communications industry as it builds toward 4G-LTE Advanced and 5G standards. We are excited to partner with Soitec in developing next-generation SOI communication solutions. It is consistent with SITRI's mission to create a collaborative R&D and commercialization environment to catalyze the growth of advanced technologies," said Dr. Charles Yang, president of SITRI.

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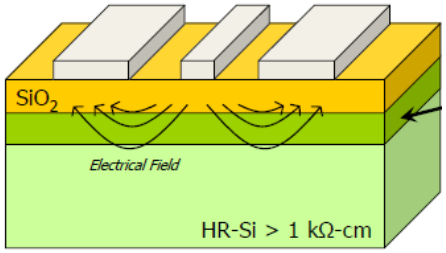
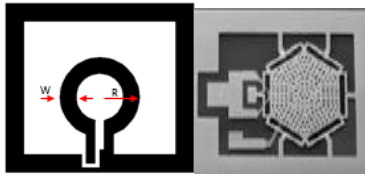
Soitec-SITRI Joint Development Program on High Performance RF SOI Technology

Joint collaboration between SITRI and Soitec for research and development of RF SOI technology solutions including device, circuit design and RF CMOS technology



Various substrates RF performance

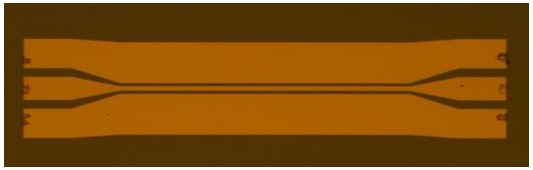


High performance passive RF Devices

RF MEMS?
III-V on Silicon?
New technologies?

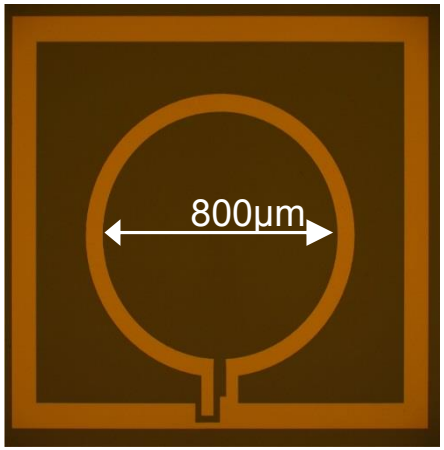
RF substrates for 5G applications

Fabricated Passive Devices on RF-SOI Substrates



W=26μm, S=12μm, L=500μm

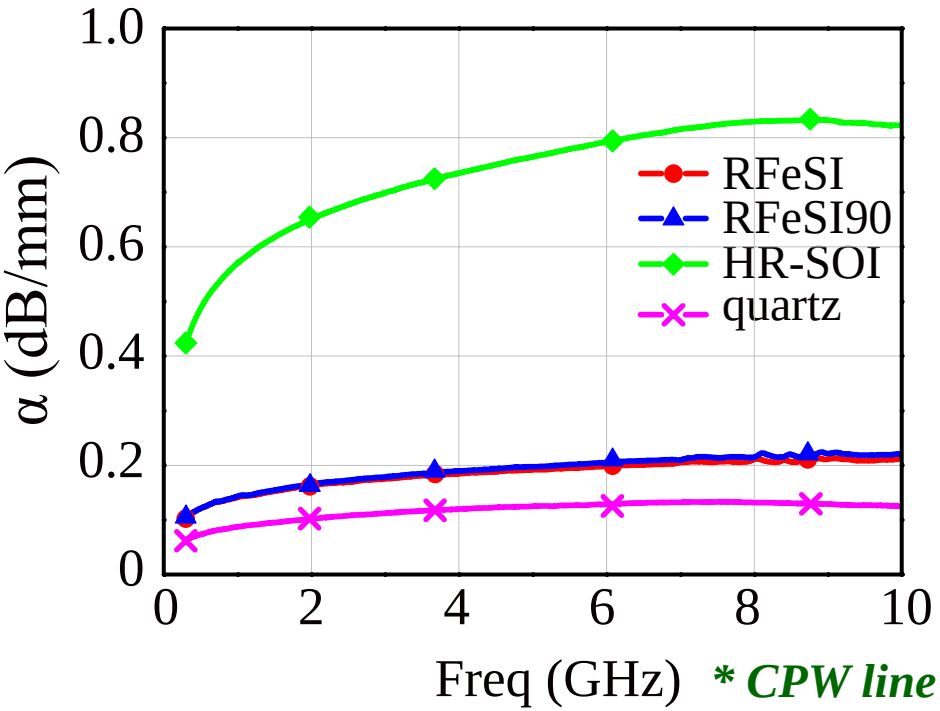
W=26μm, S=12μm, L=2176μm



Substrates	ρ (kΩ·cm) of bulk Si	ρ (kΩ·cm) bellow BOX	t_{ox}(μm)	t_{Si}(μm)
HR-SOI	5.6	NAN	0.4	725
RFeSI G1	＞10	6.5	0.4	725
RFeSI 90	＞10	16.7	0.4	725

* Metal stack is 500nm Al and 500nm Au.

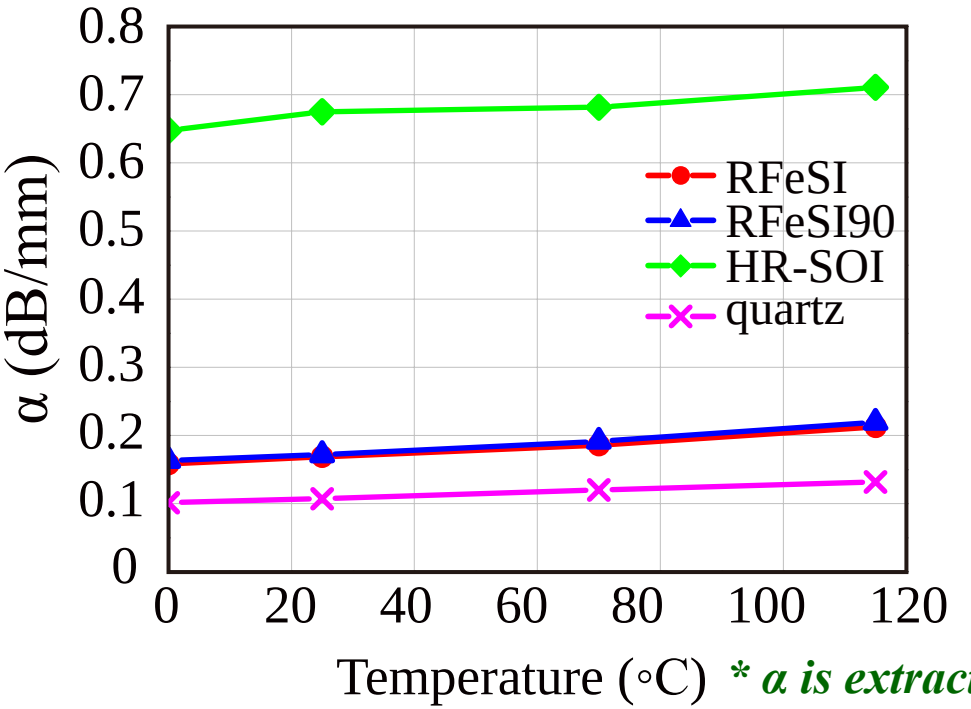
Measurement Results of CPW Transmission Lines: Attenuation Factor



** CPW line size are: 26, 12 and 208 um.*

- **RFeSI substrates present much reduced losses compared with HR-SOI substrates, while RFeSI and RFeSI90 substrates show almost same loss.**

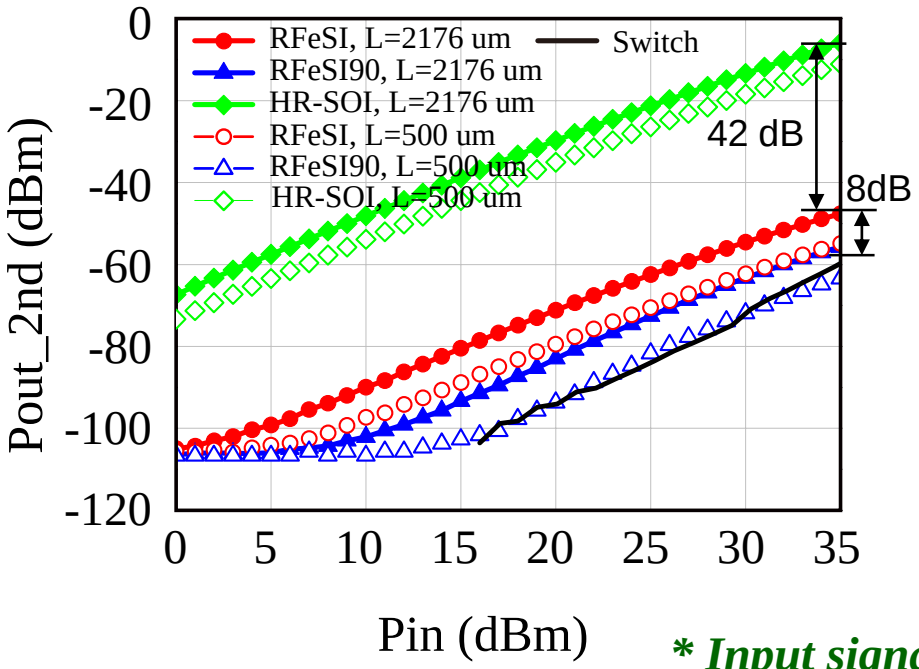
Measurement Results of CPW Transmission Lines: Temperature Effect on Attenuation Factor

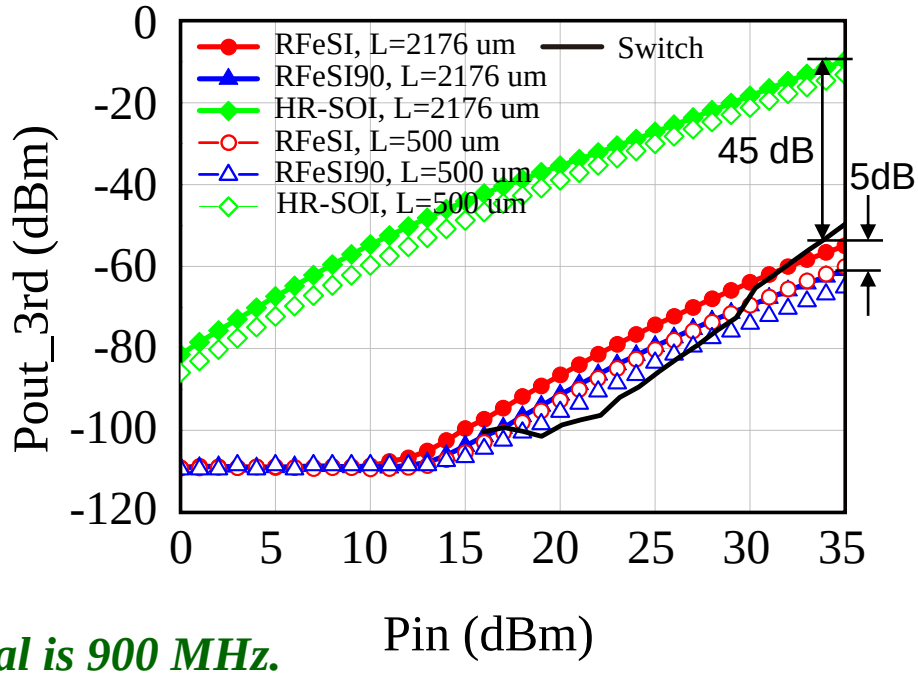


** α is extracted at 2.45 GHz.*

- **Increased α with raising temperature is predominated by the increasing metal loss.**

Measurement Results of CPW Transmission Lines: 2nd and 3rd Harmonics





** Input signal is 900 MHz.*

- CPW lines with 2176 um and 500 um length and an SPDT switch using a commercial 0.18 um RF-SOI process are compared.
- RFeSI90 substrates shows the best harmonic suppression.
- Shorter CPW lines have better harmonic suppression due to less coupling to the substrate.

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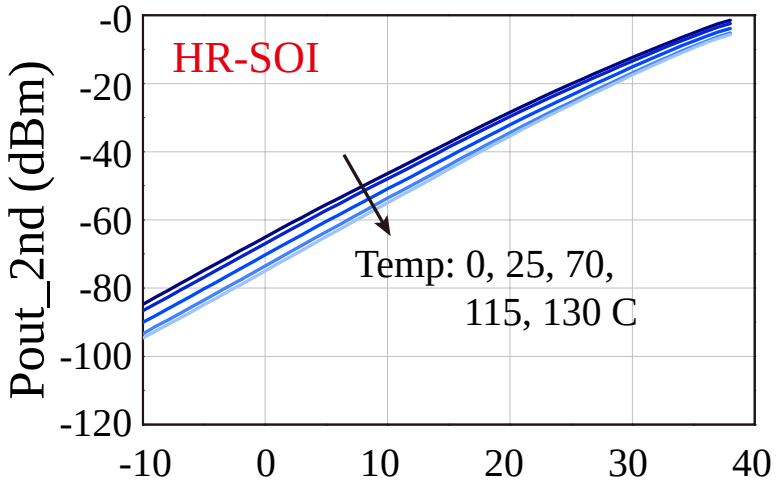
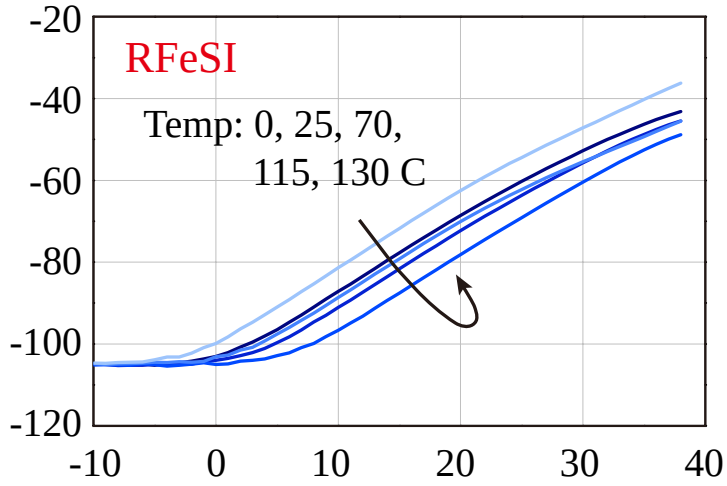
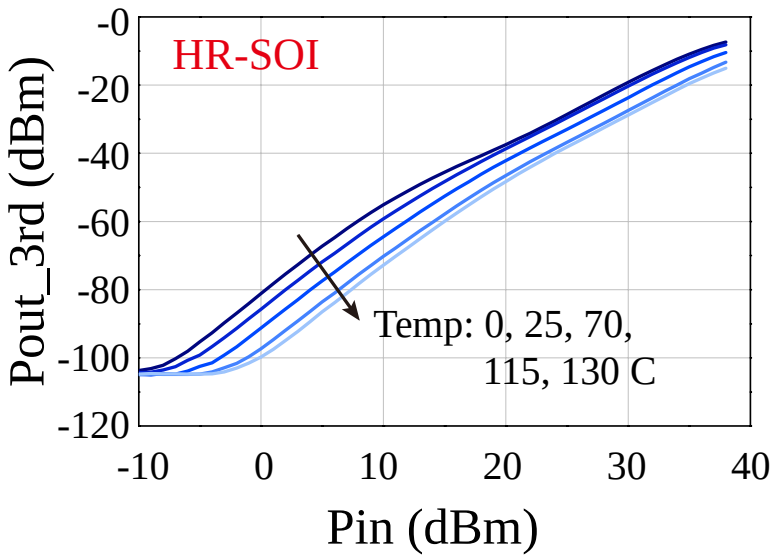
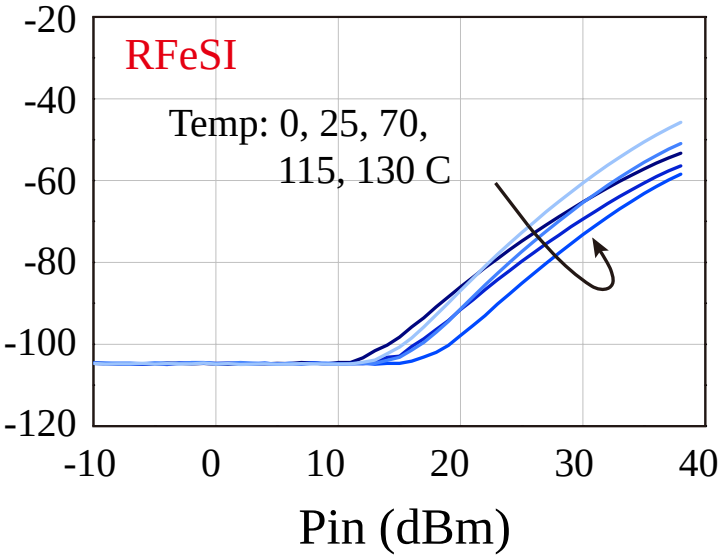
Measurement Results of CPW Transmission Lines: Temperature Effect on 2nd and 3rd Harmonics









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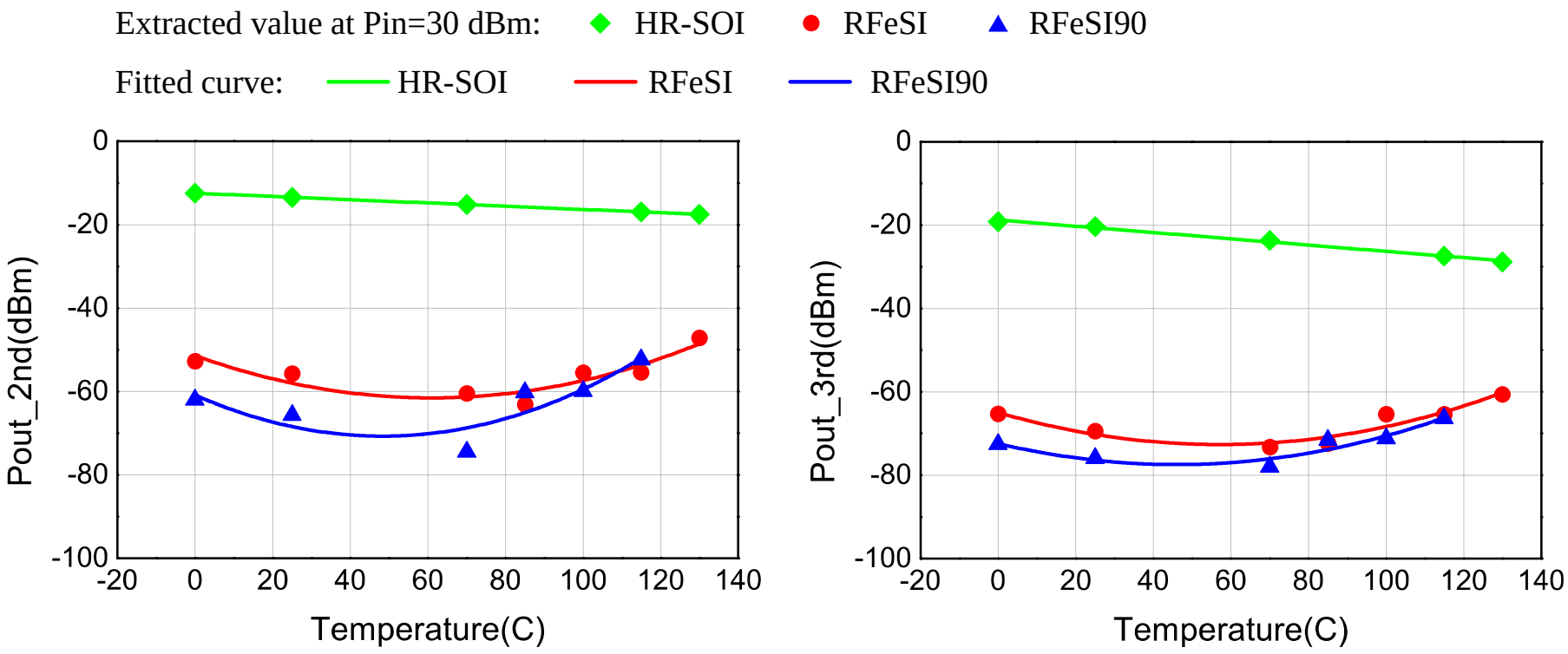
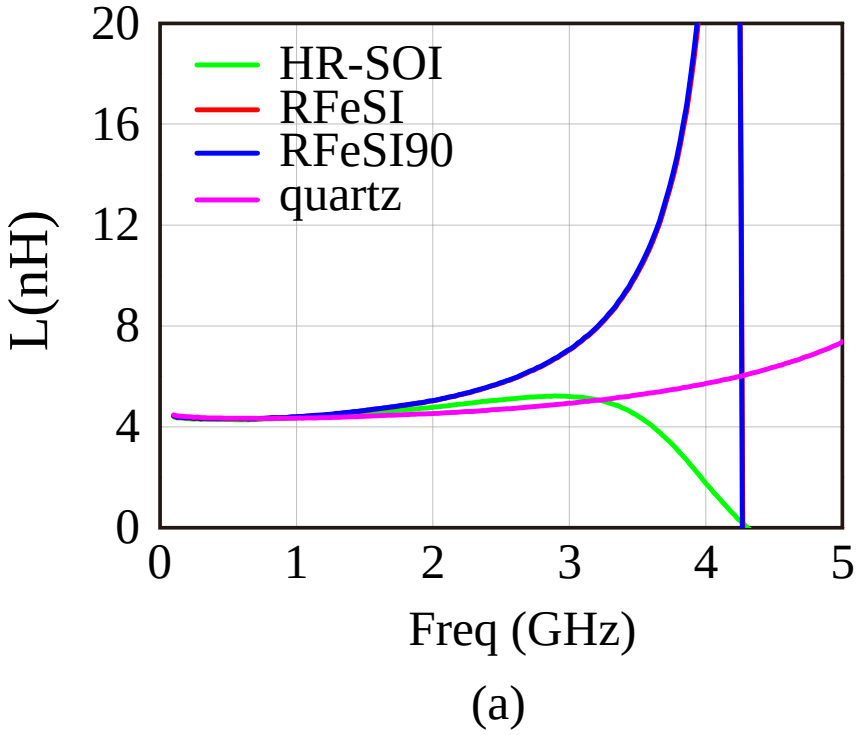
Measurement Results of CPW Transmission Lines: Temperature Effect on 2nd and 3rd Harmonics

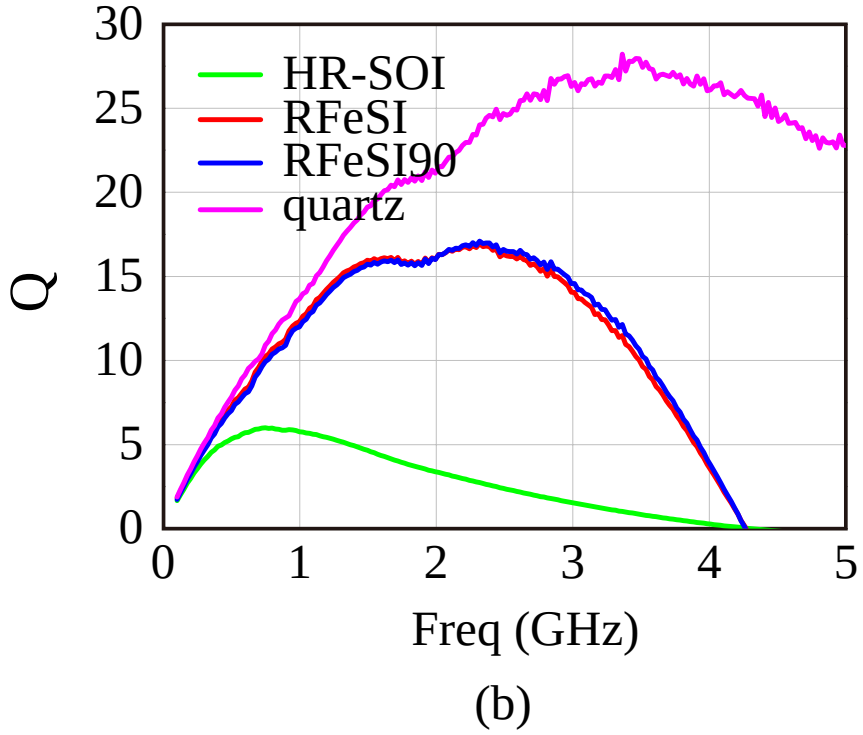


- **Extracted 2nd and 3rd harmonics when Pin=30 dBm**

Measurement Results of Spiral Inductors: Inductance and Quality-Factor



(a)



(b)

- **The inductors on RFeSI substrates show much higher Q than those on HR-SOI ones, while RFeSI and RFeSI90 substrates show similar inductor performance.**

Conclusion

- The CPW lines fabricated on RFeSI and RFeSI90 substrates show superior RF performance, i.e. lower attenuation and harmonics, compared to those on the HR-SOI substrate.
- α increases with increasing temperature for both HR-SOI and RFeSI substrates.
- RFeSI90 substrates show the best harmonic performance among HR-SOI, RFeSI and RFeSI90 substrates.
- The spiral inductors fabricated on RFeSI and RFeSI90 substrates present much larger Q than those on the HR-SOI substrate.

Thank You !

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