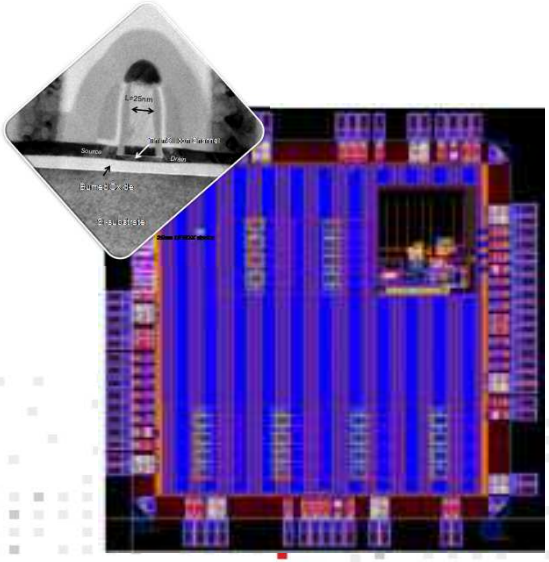

FDSOI TECHNOLOGY: GENERAL OVERVIEW & LOW-POWER DESIGN

SITRI FDSOI workshop l 08/09/2016

OUTLINE

- **FDSOI technology overview**
  - From bulk to UTBB-FDSOI
  - FDSOI technology flavors
  - Comparison between the different options
- **UWVR & ULV applications**
  - FRISBEE UWVR test chip & design techniques
  - UWVR memory
  - ULV memory
  - ULV design gain

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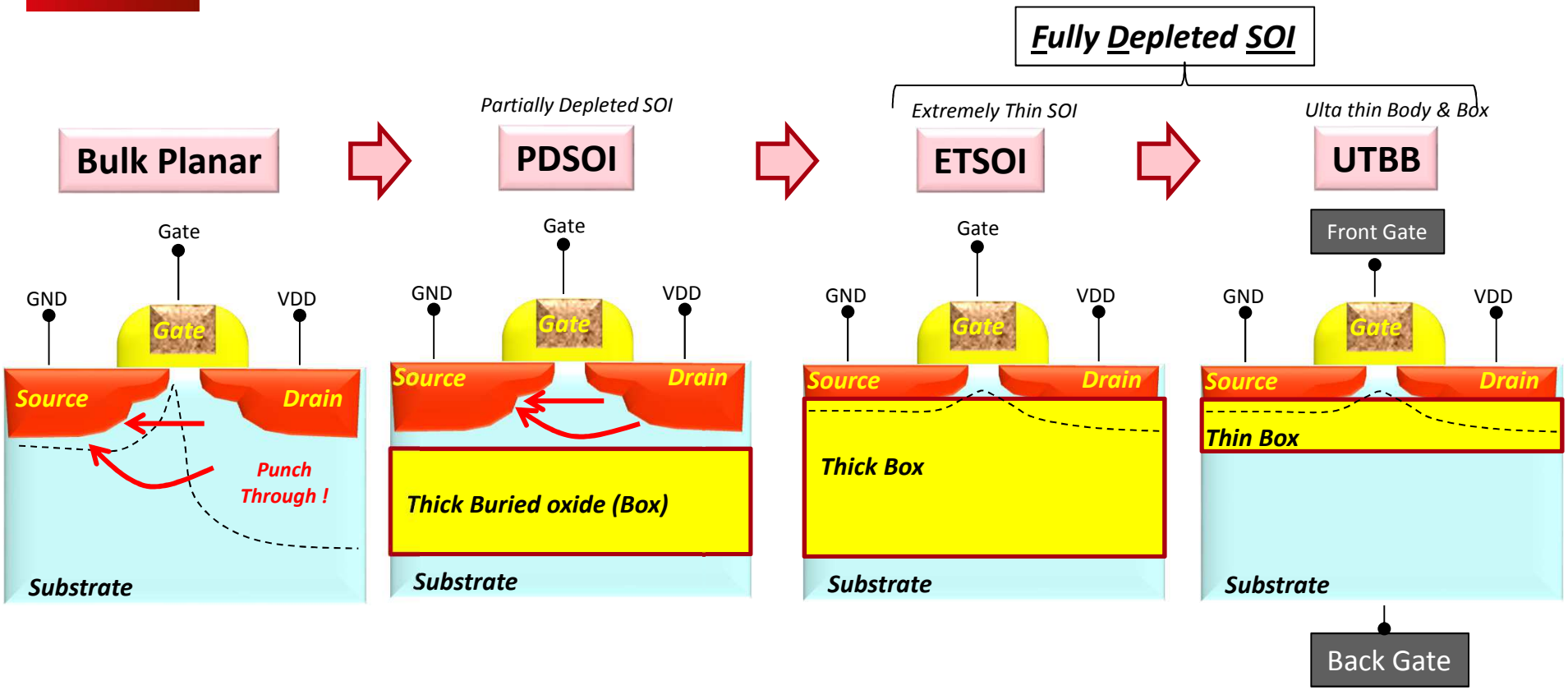
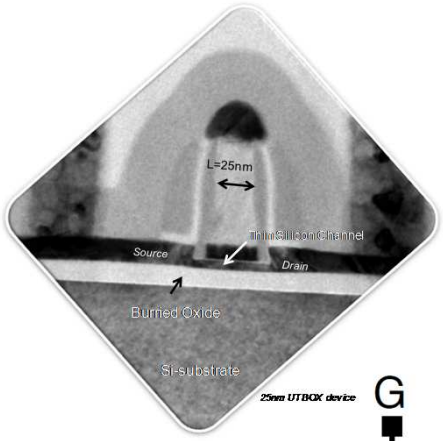
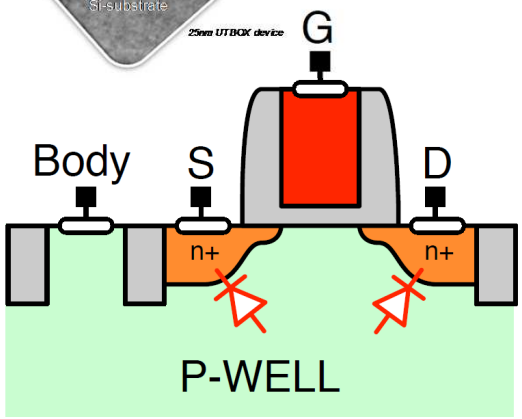
SOI ARCHITECTURES LANDSCAPE



Bulk Planar	PDSOI	ETSOI	UTBB
Low Electrostatic performance Low VT modulation capability	Low Electrostatic performance Low VT modulation capability	Good Electrostatic performance Low VT modulation capability	Good Electrostatic performance Efficient VT modulation capability

CMOS UTBB-FDSOI DEVICES



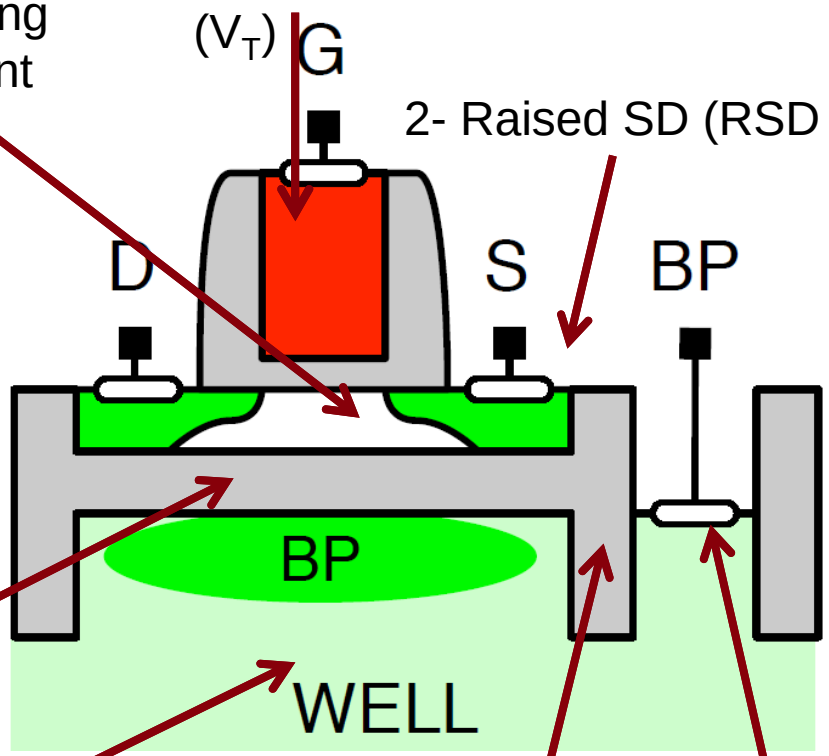


Bulk NMOS Device

3- Si-film (≈L_G/3)
No channel doping
No pocket implant

1- Gate stack
High k (C_{OX}↗)
Metal-Gate
(V_T)

2- Raised SD (RSD ↘)



4- BOX (25 nm)

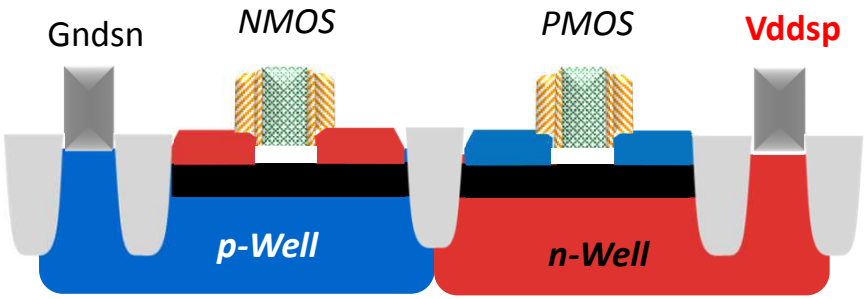
5- Back plane or WELL (V_T)

7- Isolation (STI)

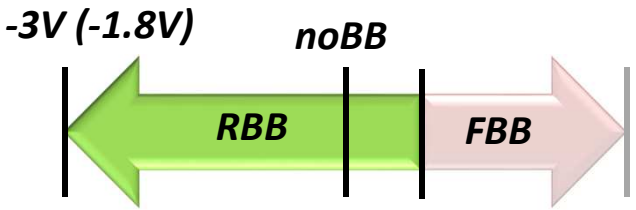
6 – Back Biasing

28FDSOI & BODY BIAS (BB) FLAVORS

Regular Well (RW) – Reverse BB

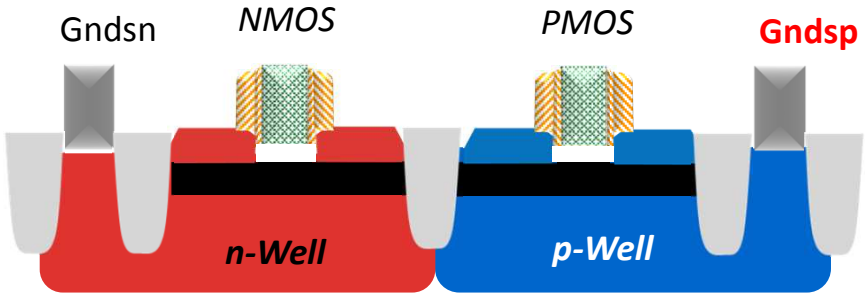


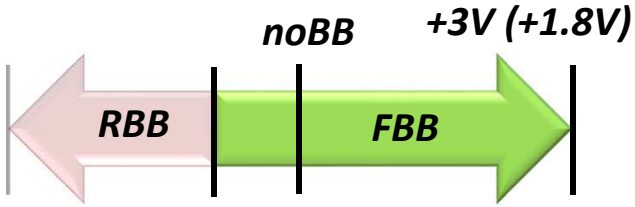
V_{th} ↑ & I_{ddq} ↓



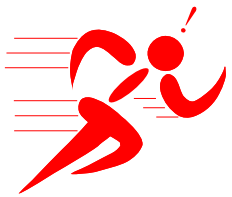
Vdd/2+ 300mV

Flip Well (FW) – Forward BB



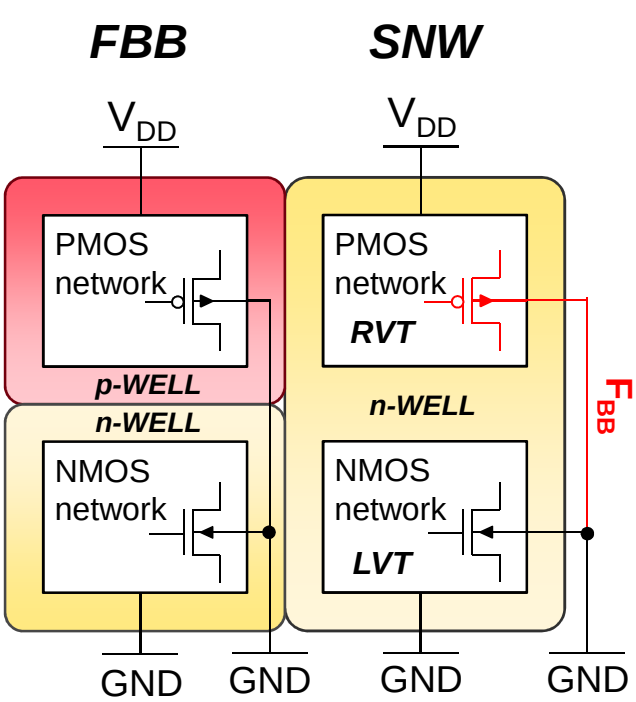


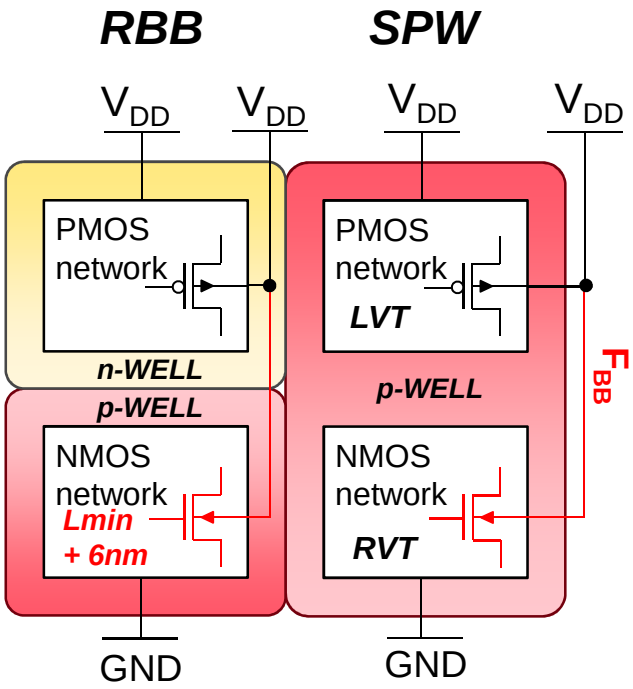
-300mV



V_{th} ↓ & I_{ddq} ↑

SINGLE-WELL OPTION



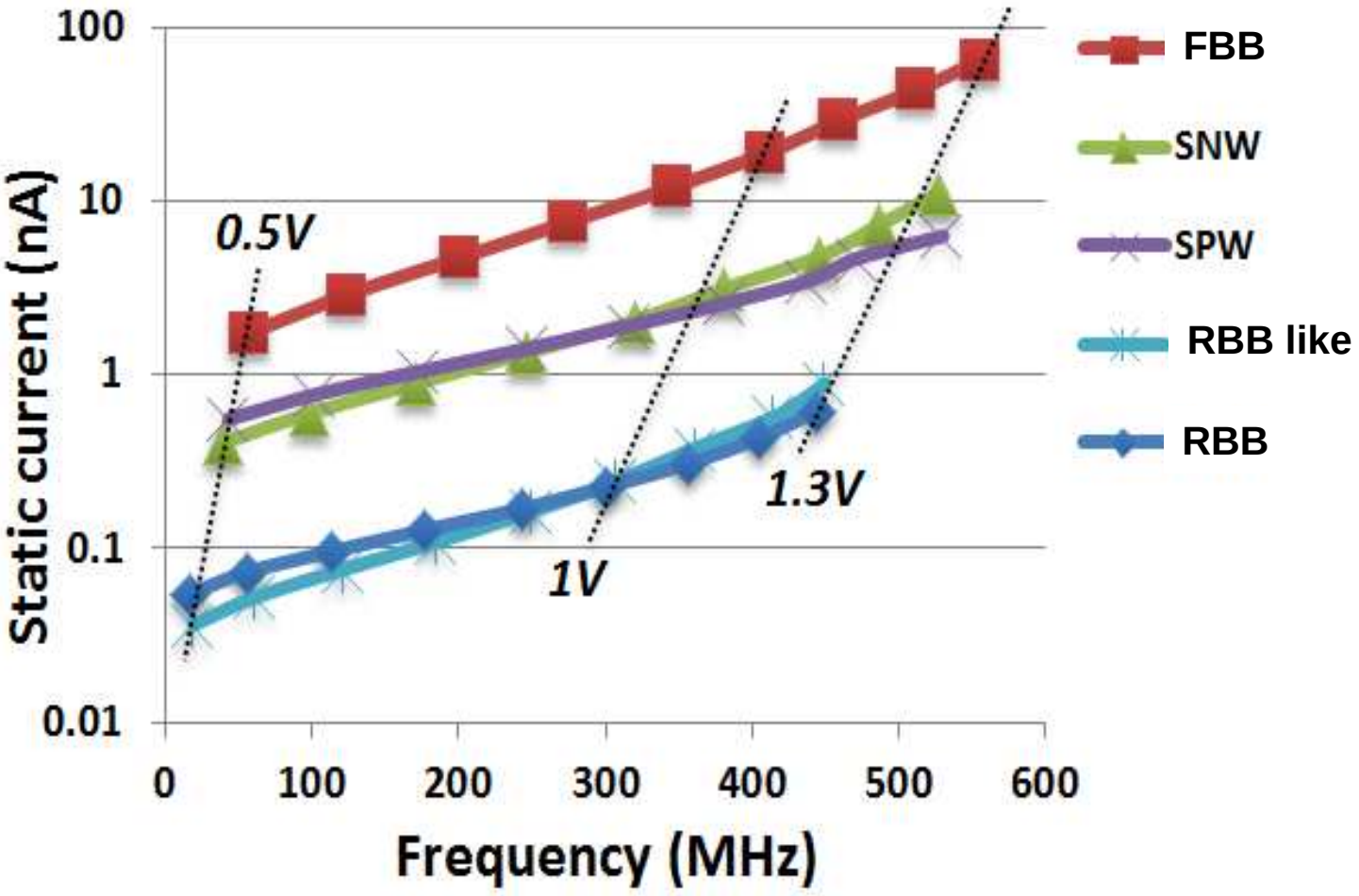


FBB & SNW co-integration

RBB & SPW co-integration

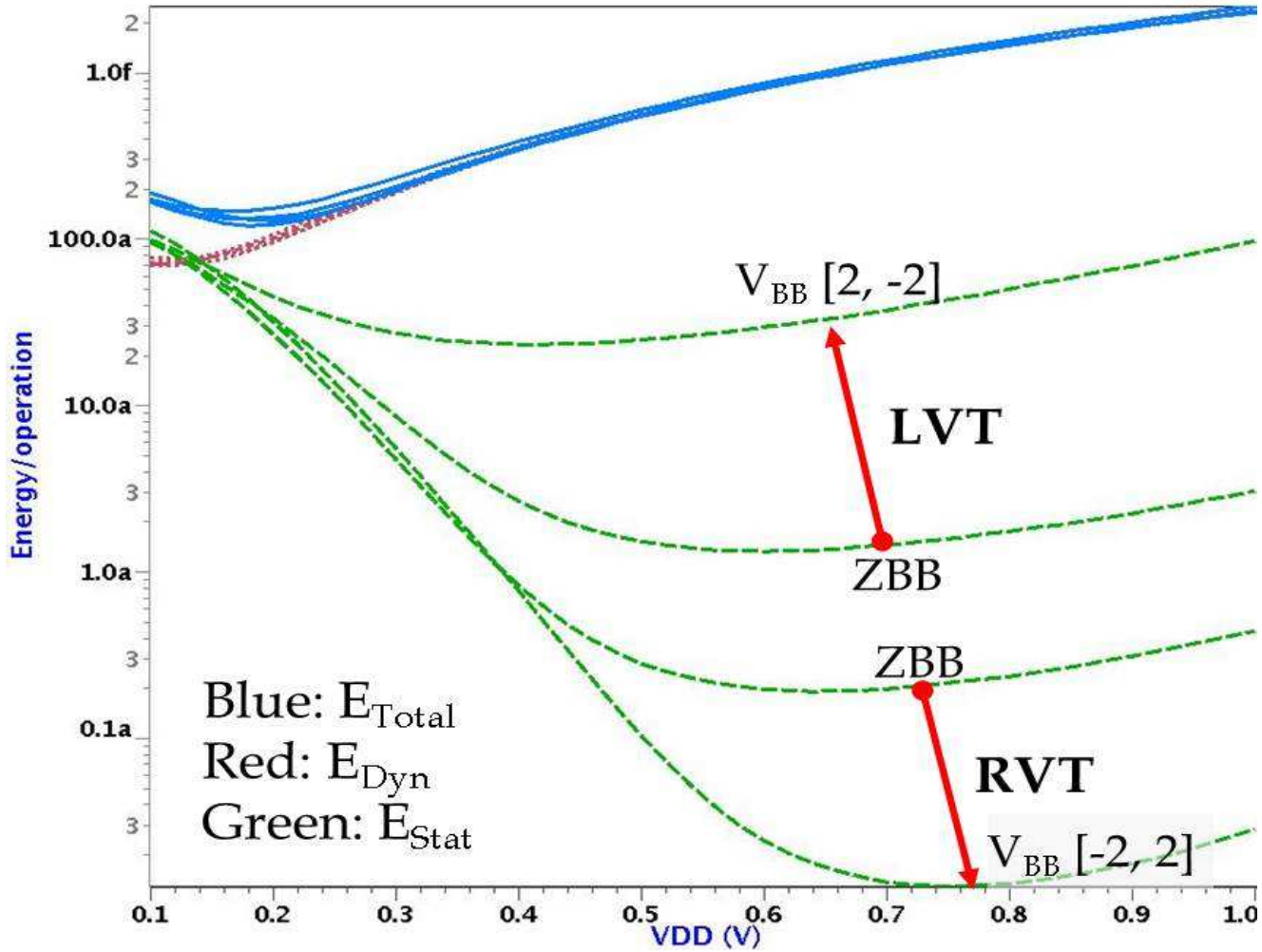
A. Valentian et al., S3S 2015

FBB/RBB/SN(P)W RELATIVE PERFORMANCES

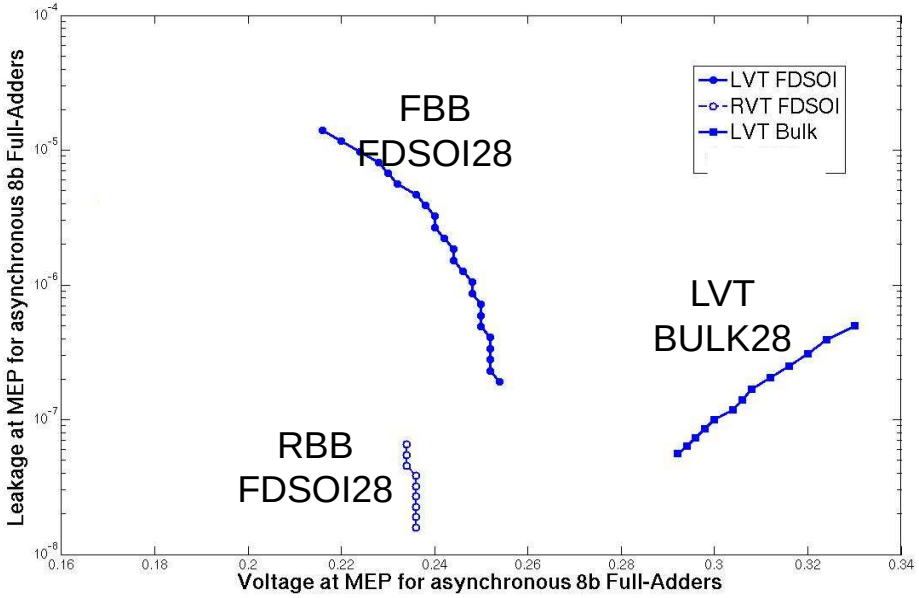


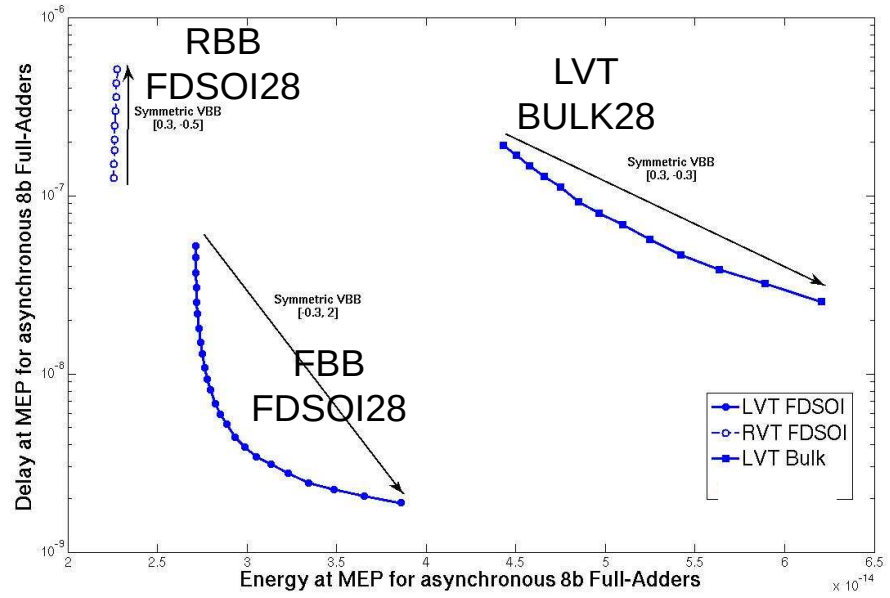
[A. Valentian et al., S3S 2015]

UTBB FDSOI AND ENERGY EFFICIENCY



FBB/RBB/BULK TECHNOLOGY COMPARISON





- RVT FDSOI-based Full Adders present less energy consumption, although the slowest behavior.
- Bulk ones show the worst overall performance.
- VBB knob allows FDSOI performance adaptation
- Better variability allows a lower Vdd operation

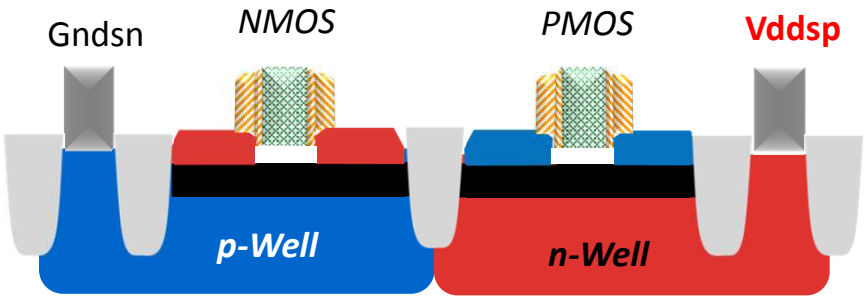
CONCLUSION: A NEW LANDSCAPE FOR DESIGNERS

- **FDSOI is a new landscape for designers, opening different optimization choices:**
  - RBB / FBB islands choices
  - Poly-biasing / single well options
  - **Dynamic** control of FBB/RBB

- **But also:**
  - New IP designs
  - Better process variability control
  - RF/analogue with best-in-class characteristics

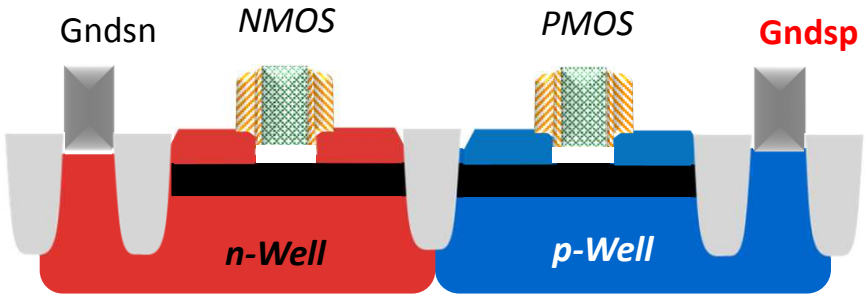
28FDSOI & APPLICATIONS

Regular Well (RW) – Reverse BB



Ultra-Low leakage
=> always-on, low performance

Flip Well (FW) – Forward BB



Energy efficiency
=> Continuum of performance (UWVR)
=> performance @ Low voltage

OUTLINE

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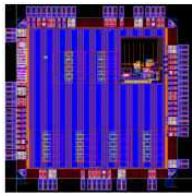
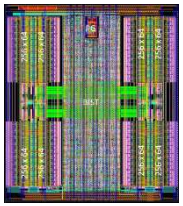
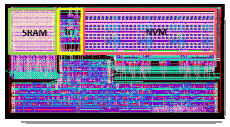
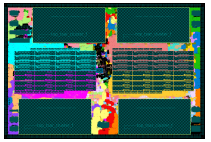
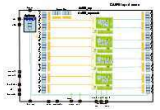
AN OVERVIEW OF FDSOI DIGITAL CIRCUITS @ LETI



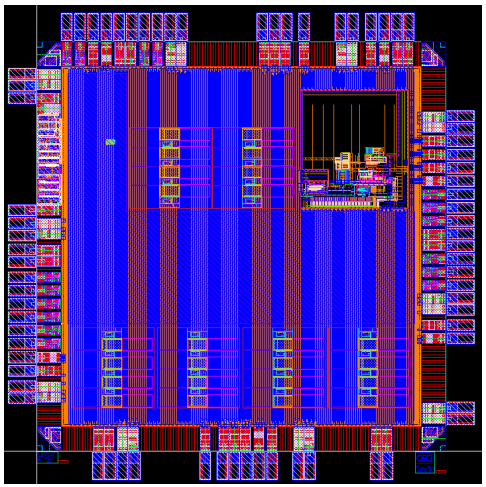



	FRISBEE	SRAM Defect	VIDOCQ	DIPMEM	SHARP	RUSH (LIOT)
Technology	FDSOI 28nm	FDSOI 28nm	FDSOI 28nm	FDSOI 28nm + RRAM	FDSOI 28nm	FDSOI 28nm
Main features	Ultra Wide Voltage Range DSP	Characterization of FDSOI Memory	Ultra Wide Voltage Range Memory	Mixing SRAM and NVM for fast switch-on/off.	Low-power multi-core	ULV design for always-on devices
Architec-ture	32-bit VLIW Serial interface Wide range FBB	1K x 32bits memory with embedded BIST	1K x 32 bits memory	Multi-banks architecture	MIPS based multi-core with L1, L2, L3 mem.	ARM M0+ core + peripherals
Design	UWVR SRAM and libraries Timing monitoring Pulsed latch FF	Embedded full characterization scheme. 6T SRAM cell, high density	8T SRAM cells. Write-assist scheme. Mixed-well logic design.	Mixed SRAM/NVM with common periphery. Context saving	3D Chiplet using 3D plugs Network-on-Chip Cache-coherency	0,5V design ULV memory
Main Results	2.6GHz@1.3V 460MHz@397 mV 370mW@1V 62pJ/cy@0.46V	Full charac. of RA, WA, WS with pulse width between 350ps and 30ns	400 mV min. Voltage 1,5Ghz @ 1 V	On/off in less than 1 µs. Zero leakage architecture when off.	800 Mhz MIPS Scalability demonstrated with 96 cores integration.	50 MHz @ 0,5V

FRISBEE: A PROTOTYPE FOR DEMONSTRATING FDSOI

- **Objectives:**
  - Ultra-Wide Voltage Range (UWVR) operation: Vdd=[0,3V-1,3V]
  - High performance
    - Fclk>2,7GHz @1,3V - Fclk>200MHz @ 0,35V
  - Power-efficiency

- **Frisbee Characteristics:**
  - 32-bit data-path VLIW DSP (FFT 1024)
  - UWVR 8T SRAM cuts (1Kx32) with read/write assist
  - FBB/RBB IOs delivering from -2V to 2V
  - UWVR standard cells (with 2 different poly-bias)
  - Pulsed latches for high performance FF
  - Timing margin reduction mechanism implemented (fault detectors, replica paths, fine-grain clock generator)

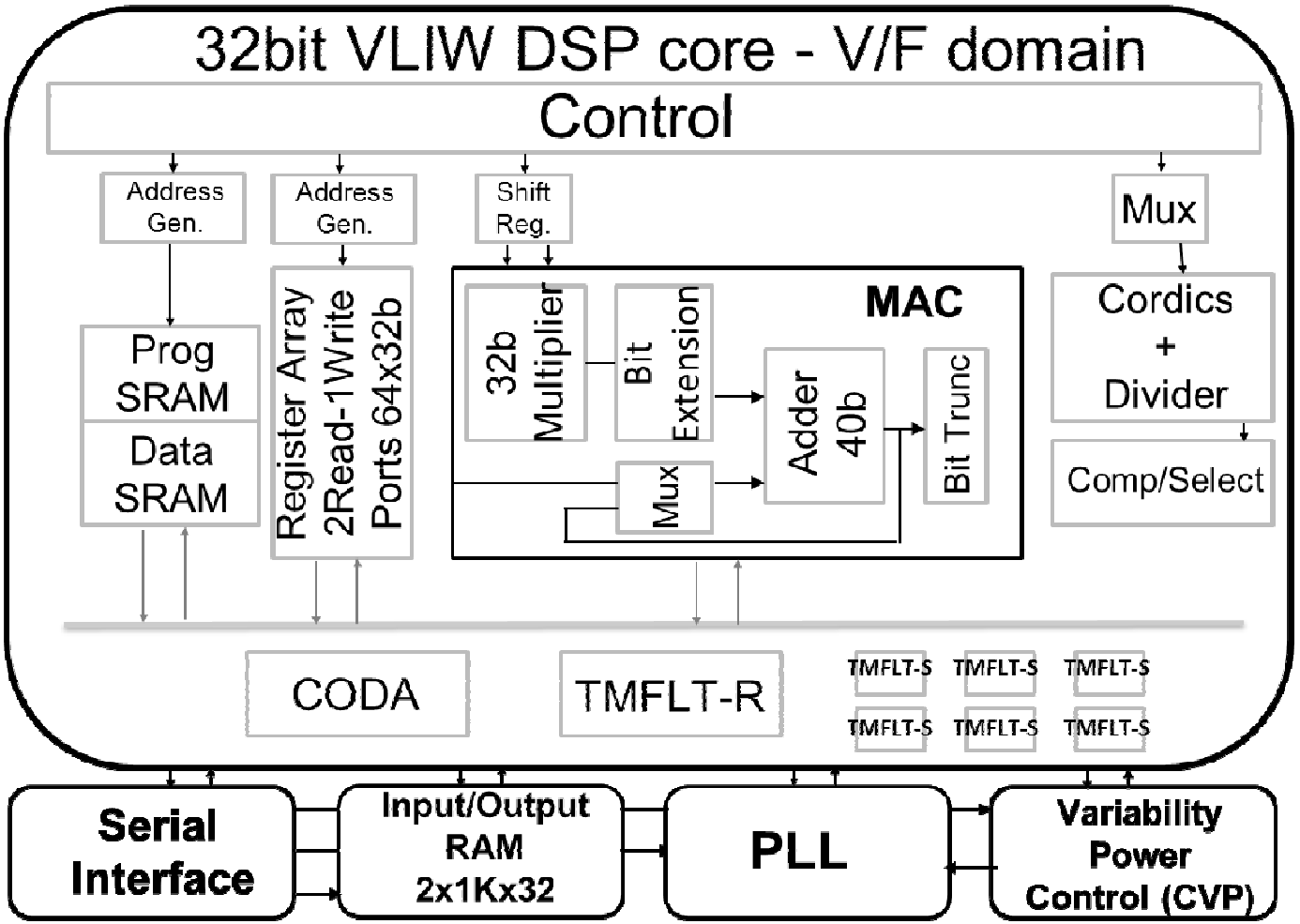


FRISBEE layout

ISSCC'14, JSSC'15

- FDSOI 28nm FlipWell
- Area = 1 mm²
- Gate nb = 2 Millions

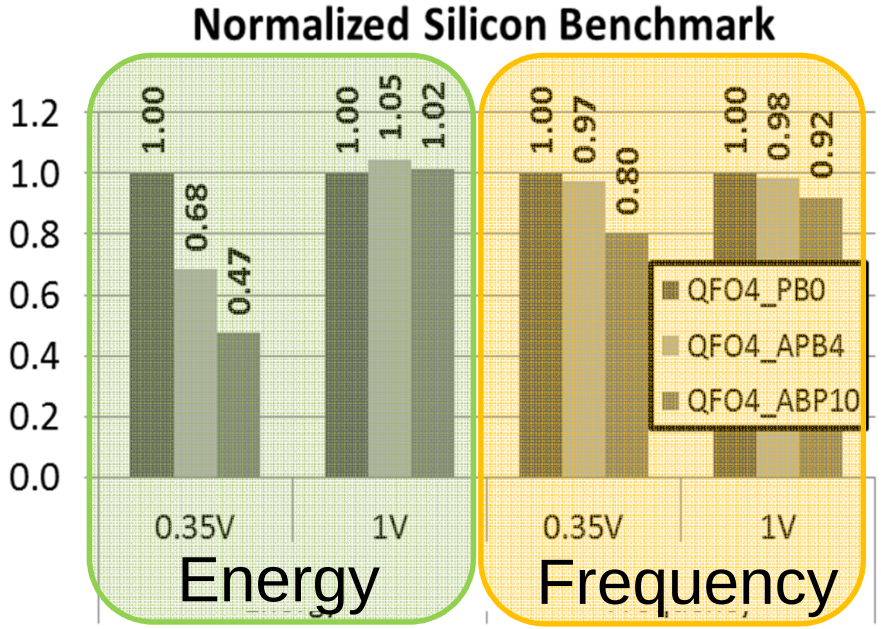
FDSOI APPLIED TO AN UWVR DSP

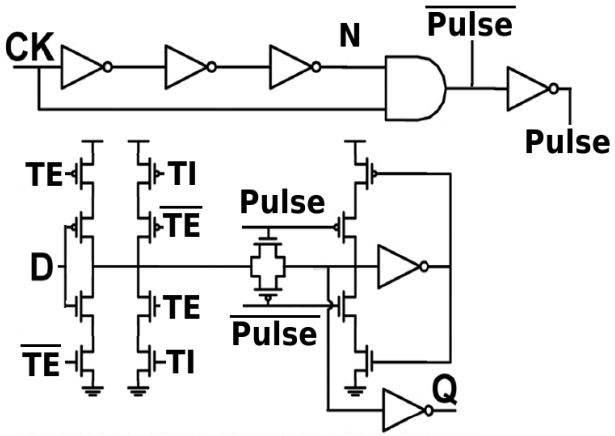


[Beigne et al. JSSC 2015]

FDSOI BENEFICE FOR ASYMMETRIC GATES

- Asymmetric PB in library cells allows UWVR optimization
- New FF designs regain interest: Pulsed-latch



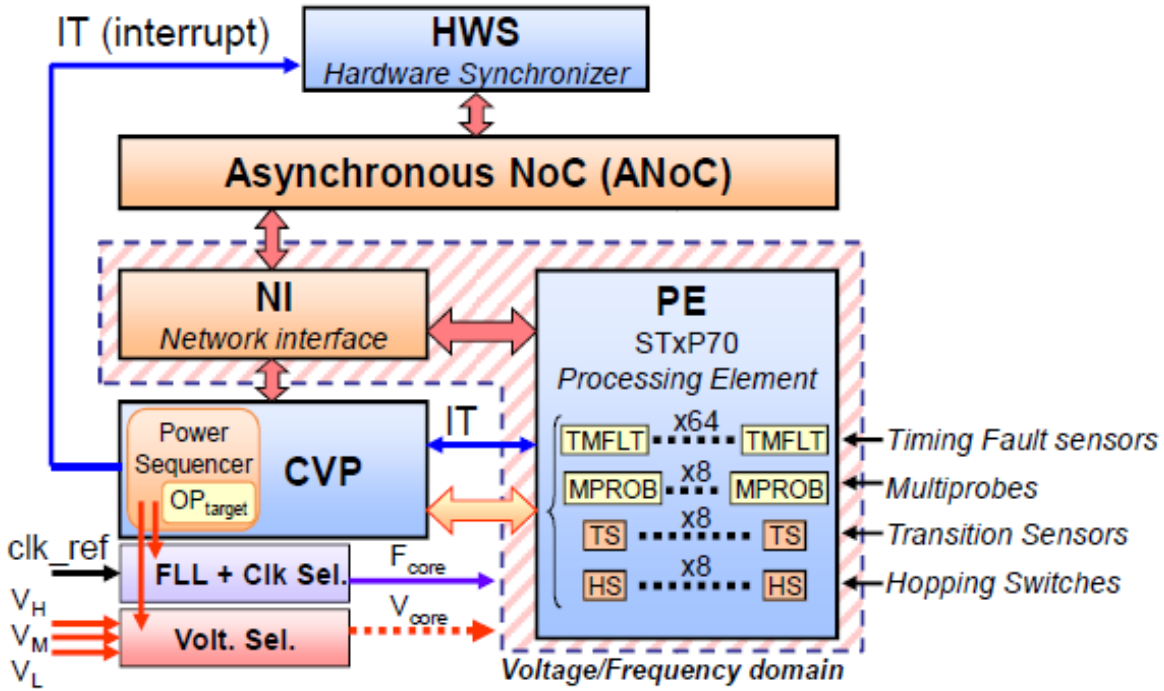


TGPLmuxScan

	D-to-Q (ps)	Egy/cycle (fJ)	Area (µm²)
ST C2MOS	117.5	6	4,41
ST SA	46.5 (- 60 %)	12.5 (+ 208 %)	6,85 (+ 55 %)
TGPLMuxScan	30.5 **(- 74 %)**	7.2 **(+ 20 %)**	4,73 **(+ 7 %)**
TGPLMuxClk	26 (- 78 %)	9.1 (+ 56 %)	5,06 (+ 14 %)

VARIABILITY / POWER CONTROL IN FDSOI : ADVANTAGES

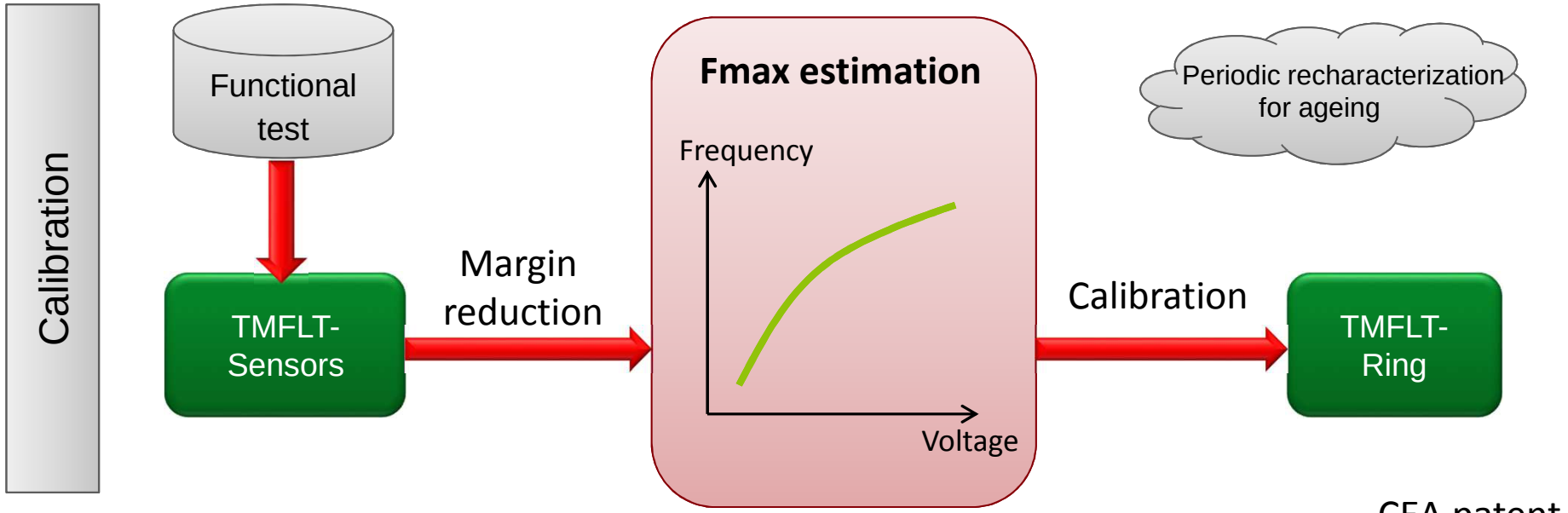
- **FDSOI allows running @ large voltage range**
- **FDSOI has reduced variability compared to bulk**
  - Larger energy or performance gains promises
- **LETI has developed a full methodology for getting benefits or this advantage with dedicated IPs**

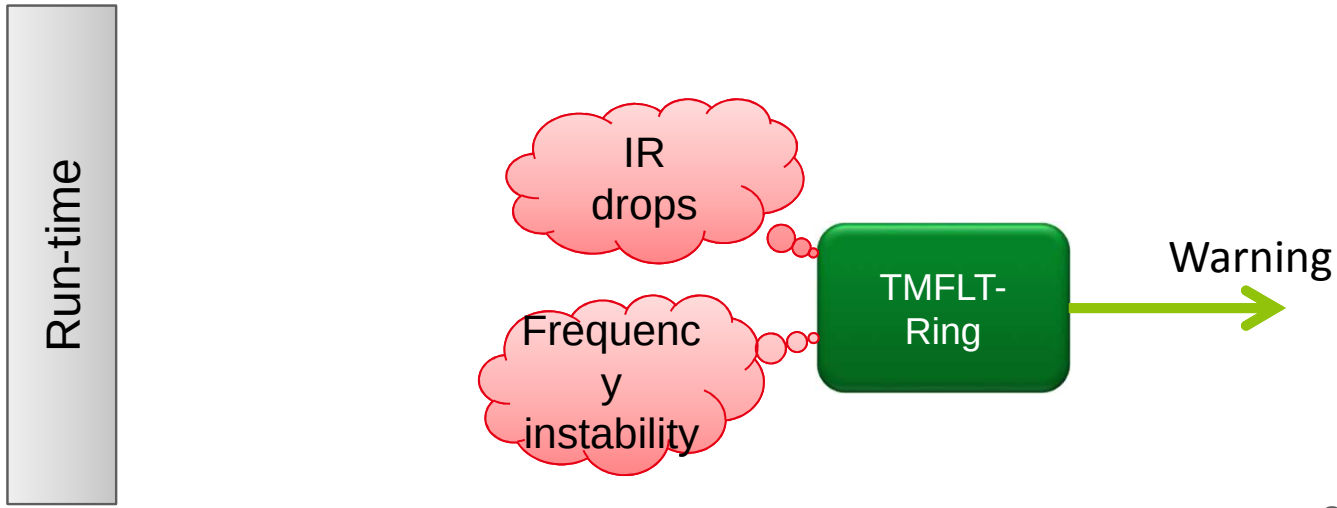


TIMING-FAULT SENSING METHODOLOGY OVERVIEW

- **Estimate and track the Fmax on Wide Voltage Range**
- **Generate statistics in order to minimize the detection margin**
- **Avoid pushing the IP to timing failure**
  - Avoid recover-after-error mechanism (Razor)
- **Reduced number of sensors (low area overhead)**
- **Without test-time overhead**
- **The characterization done in-situ (final product)**
- **Re-characterize periodically the circuit to compensate the ageing**

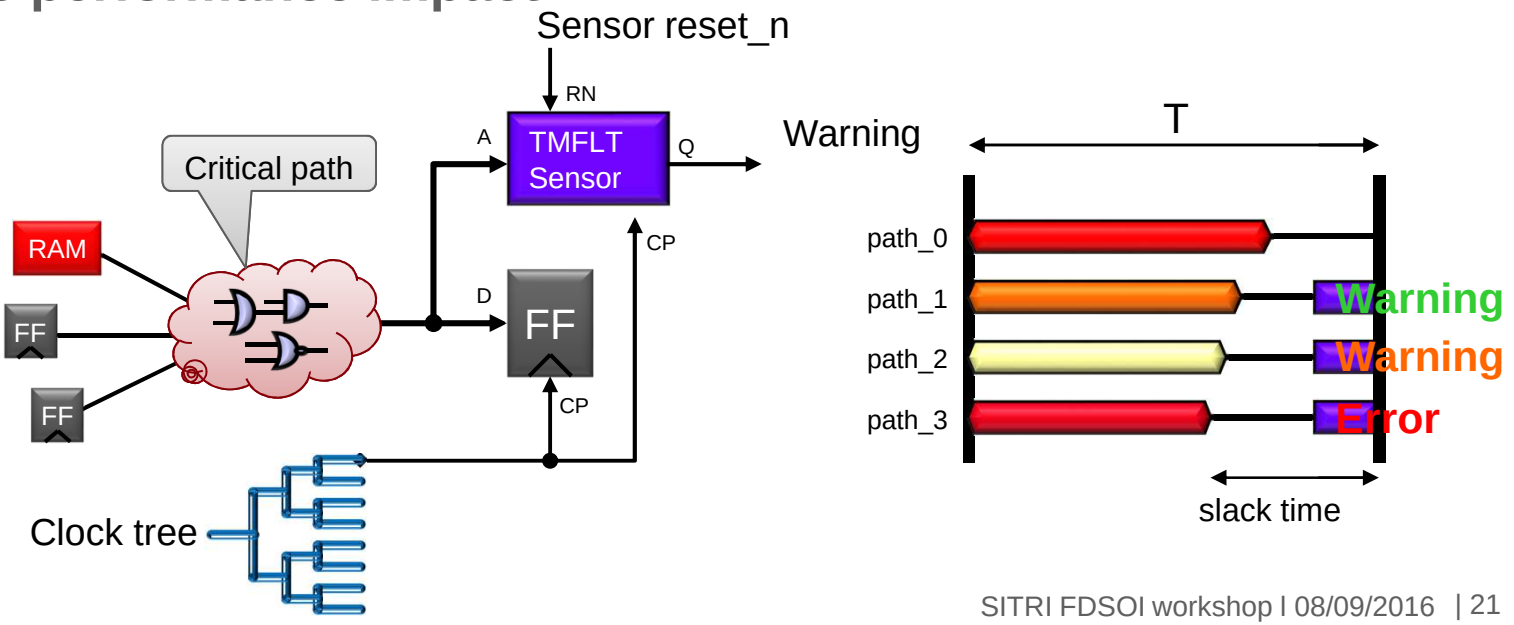
TMFLT METHODOLOGY





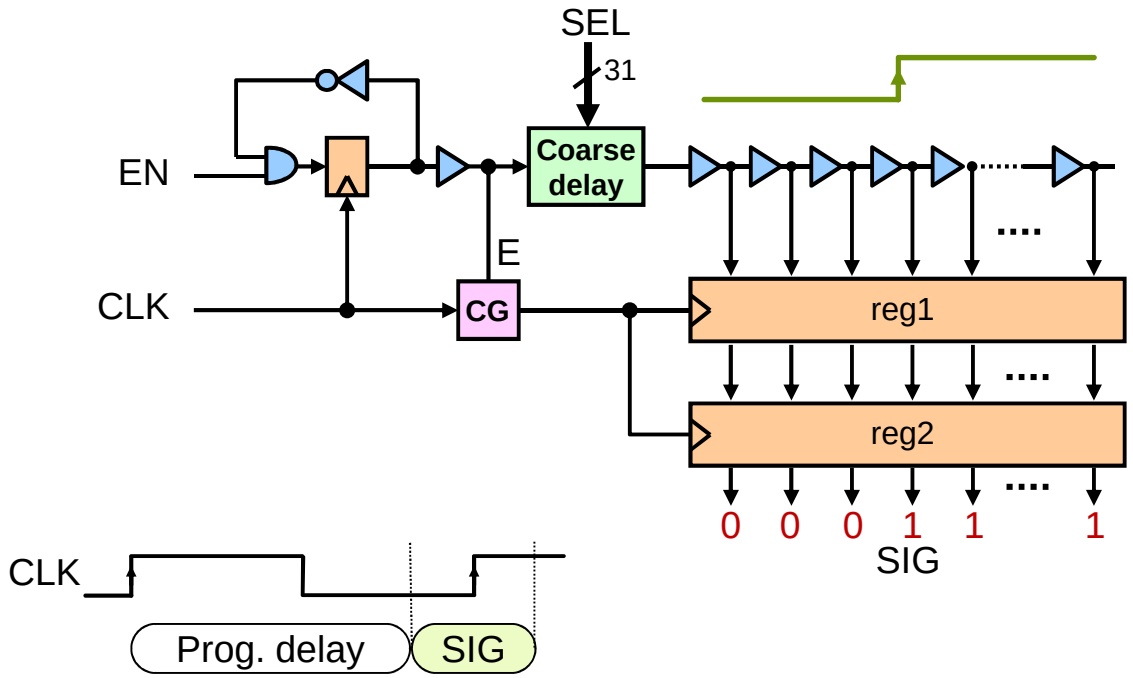
TIMING FAULT SENSOR

- Similar approach to Canary Flip-Flop
- It uses a large detection window
  - Anticipate the error detection instead of just detect the error
  - Therefore, a non-critical path can be used to anticipate the errors
- No need to instrument the most critical paths of the circuit
- Reduced number of sensors
- Low area footprint = equivalent to 2 FF, integrated as standard cells
- Negligible performance impact



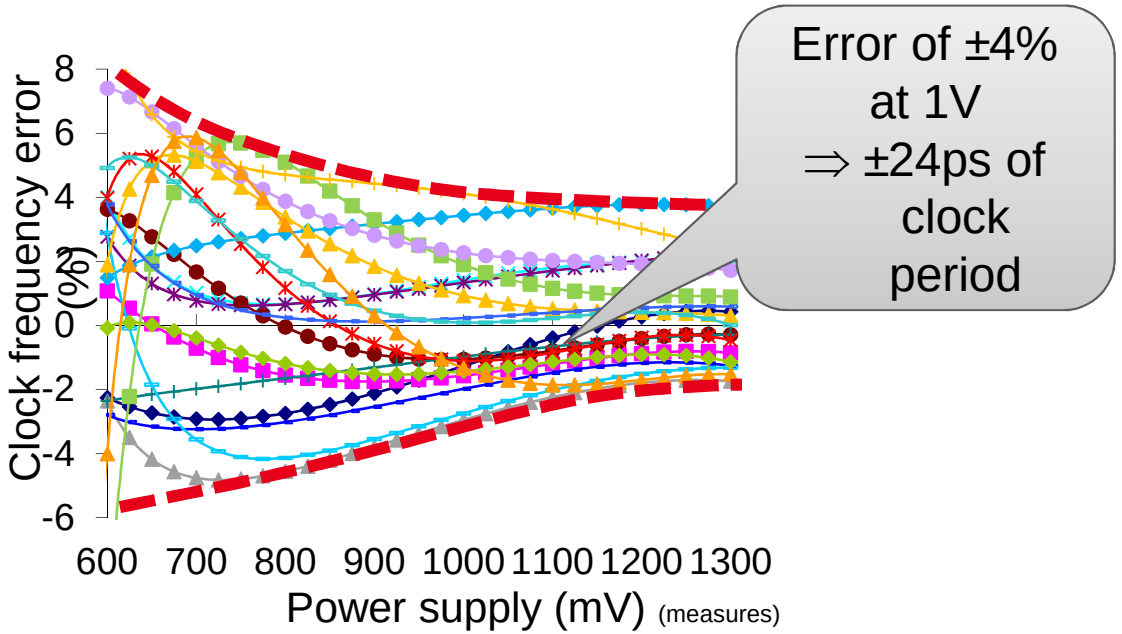
TMFLT RING

- Based on a time-to-digital converter, it measures the propagation time trough a programmable delay element and compares it with the clock period
- One measure every two clock cycles
- 300 µm2 in FDSOI 28nm



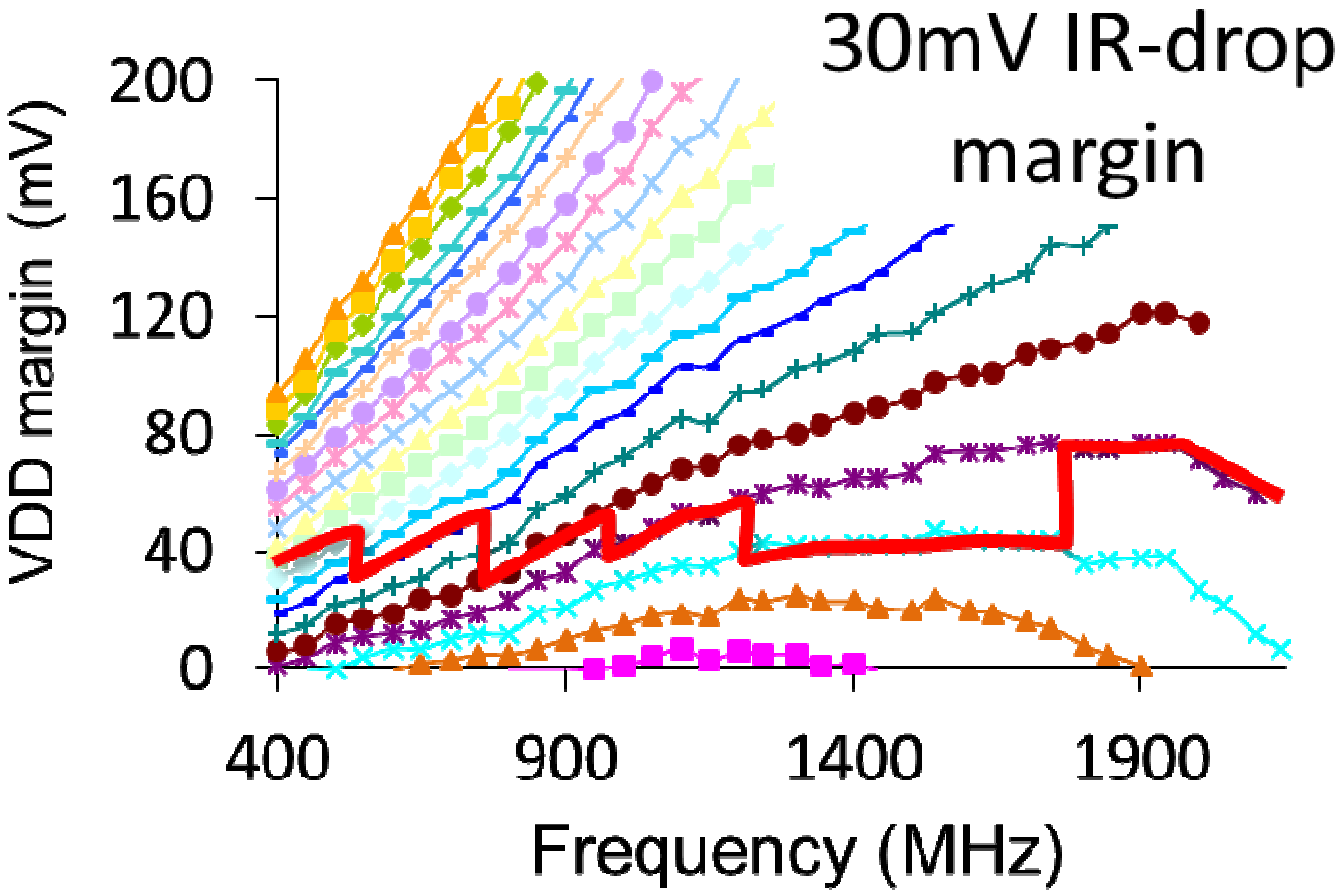
TMFLT MEASURES

- Measures on a 28nm FDSOI circuit (Frisbee)
- Nominal clock frequency 1.6GHz at 1V
- Using 21 dies on 3 wafers
- Only 10 TMFLT sensors were used
- Estimation error between the real and the estimated Fmax of the circuit:

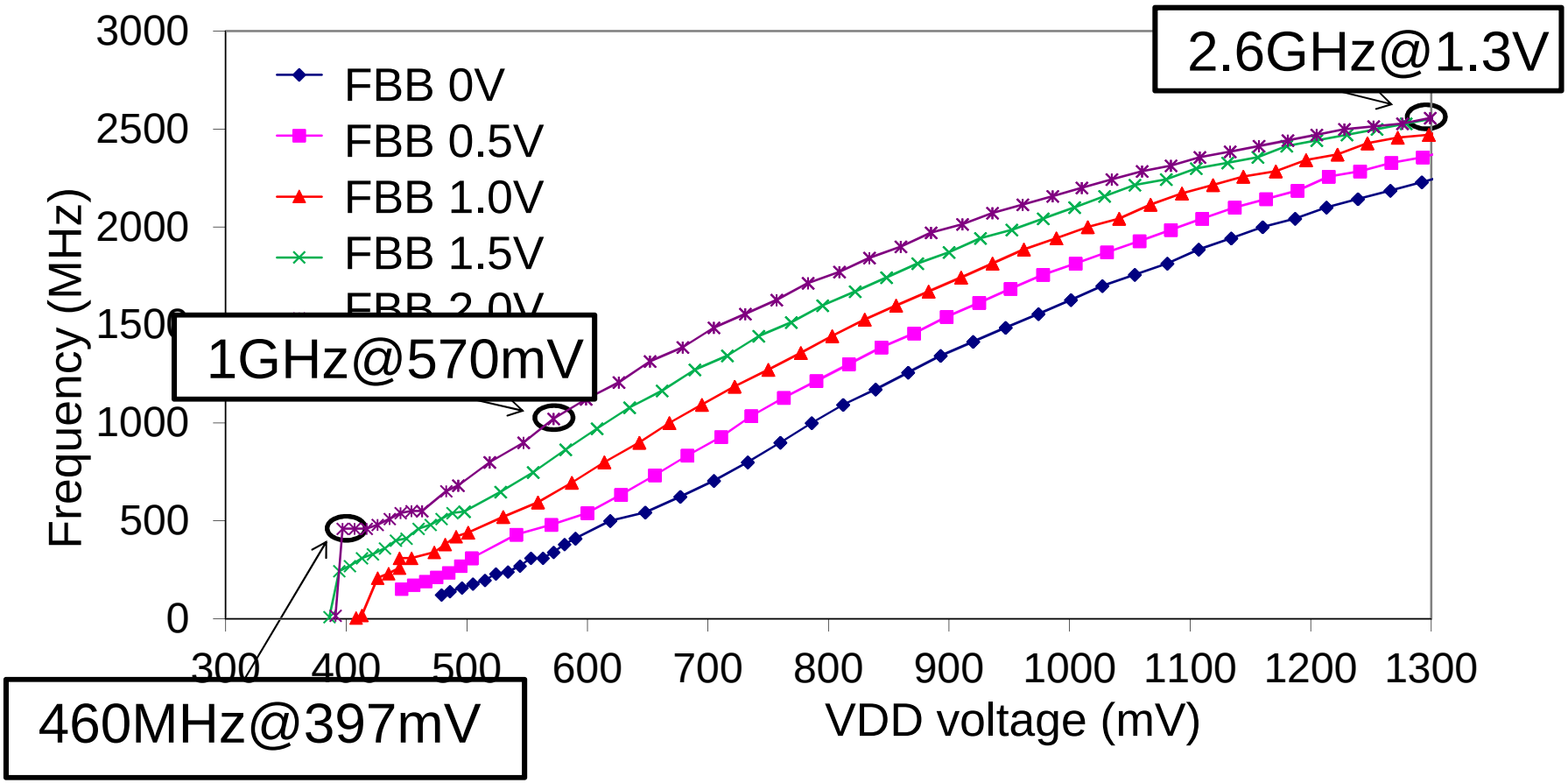


Beigne, E. et al., "A 460 MHz at 397 mV, 2.6 GHz at 1.3 V, 32 bits VLIW DSP Embedding F MAX Tracking," Solid-State Circuits, IEEE Journal of , vol.50, no.1, pp.125,136, Jan. 2015

VARIABILITY / POWER CONTROL IN FDSOI : RESULTS

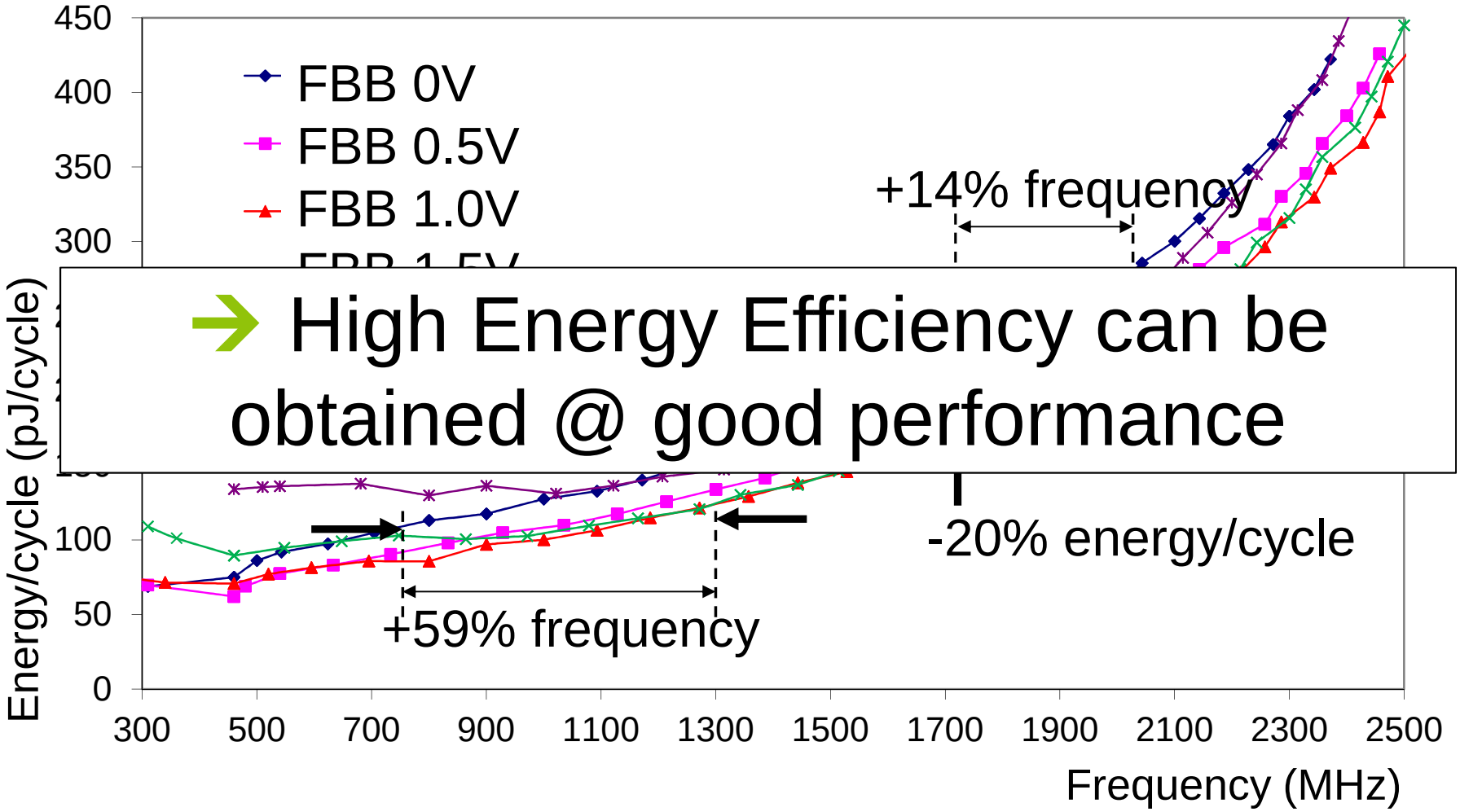


FDSOI DESIGN: F/VDD/VBB CHOICES



[Beigne et al. JSSC 2015]

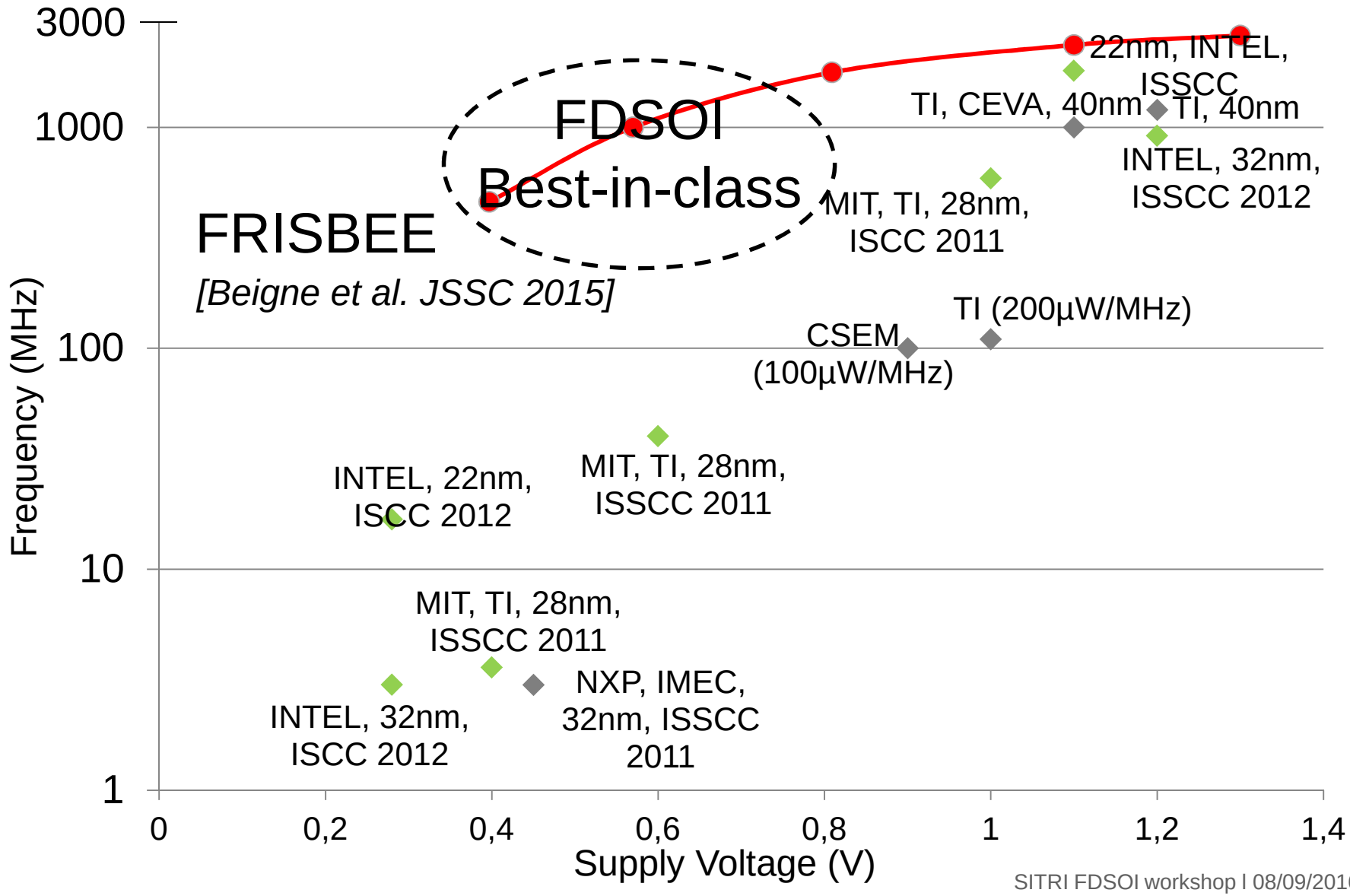
FDSOI DESIGN: BEST ENERGY EFFICIENCY POINT



➔ High Energy Efficiency can be obtained @ good performance

[Beigne et al. JSSC 2015]

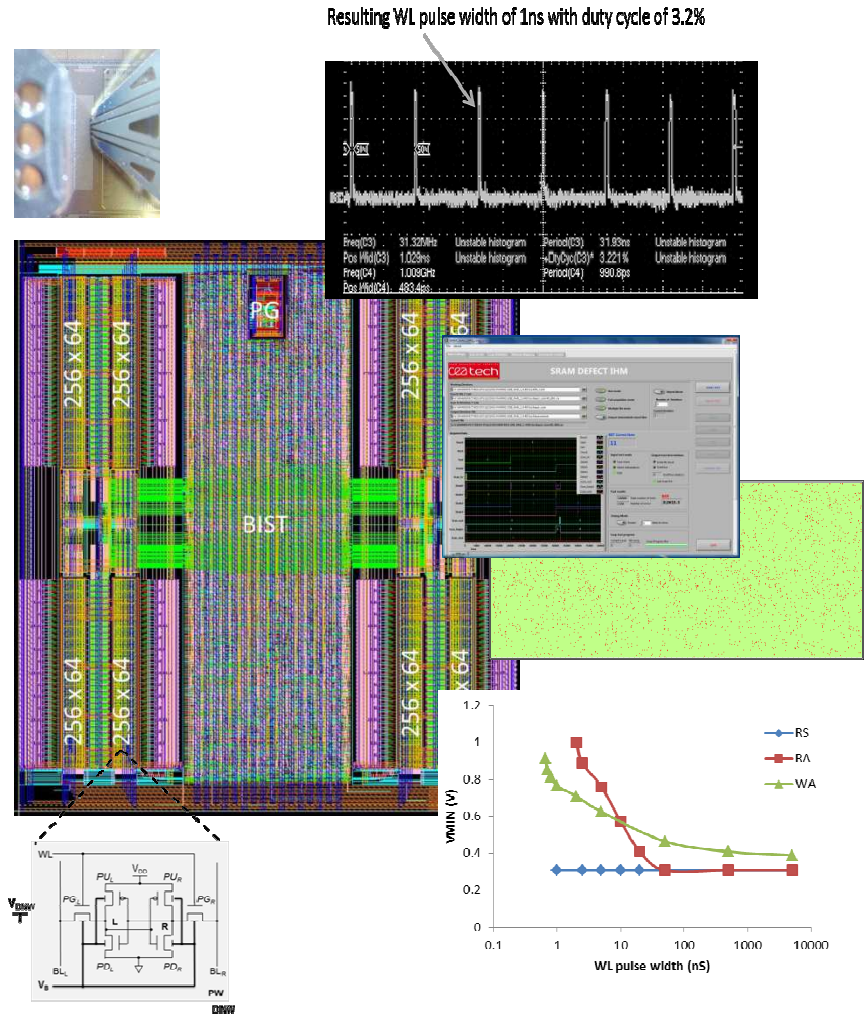
FDSOI POSITIONING WRT STATE-OF-THE-ART



FRISBEE: SUMMARY OF GAINS

- **Technological gains (compared to Bulk):**
  - Frequency: +90% @Vdd=1V, +800% @Vdd=0,5V
  - Energy: -60% @ same frequency
- **Circuit techniques gains:**
  - 8T SRAM (@Vdd=0.3V):
    - Write margin (µ/σ): 8,75 *(instead of 1.1)*
    - SNM (µ/σ): 5 *(instead of 1.2)*
  - Pulsed-Latch:
    - 3x faster than conventional Master-Slave Flip-Flop
- **Methodology gains**
  - Reduction of timing margins:
    - Frequency gain up to 25%, energy gain up to 45% (compared to WC design methodology)

FDSOI MEMORIES: SRAM DEFECT



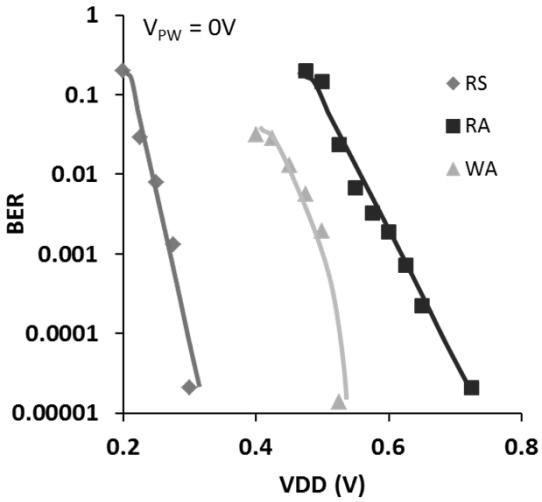
- Objectives :
  - Characterize SRAM cut perf.
  - Characterize SRAM bit cell perf.
  - Track small defects (RTN, Aging)
  - Extract yield vs. VDD & FREQ
- Design:
  - ST 28nm 5U1x 2T8x LB
  - 65kb SRAM (x2) + BIST + PG
  - 0.120µm² HDLL 6T SRAM cell
  - Pulse width: 350ps up to 30ns

➲ **Static and Dynamic characterization**

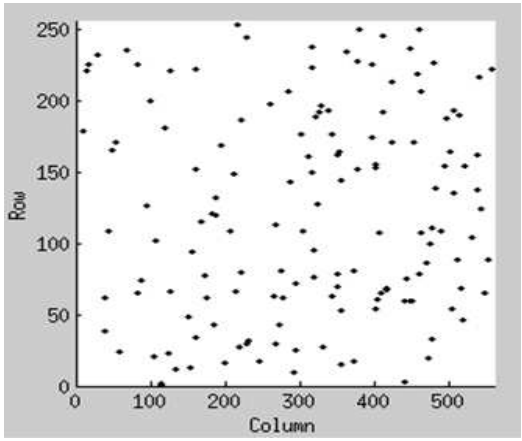
MEMORY SILICON DIAGNOSIS

Photograph

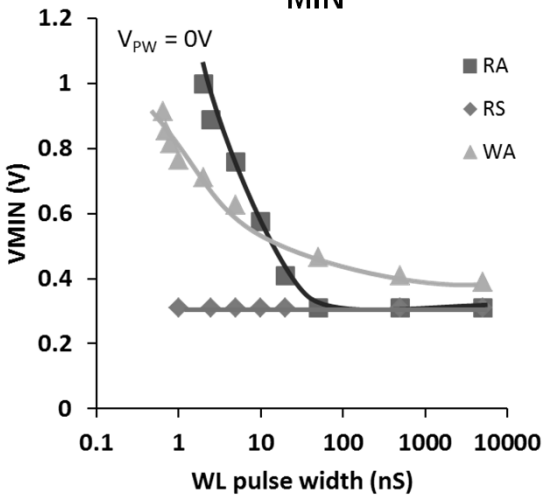
BER vs V_{DD}



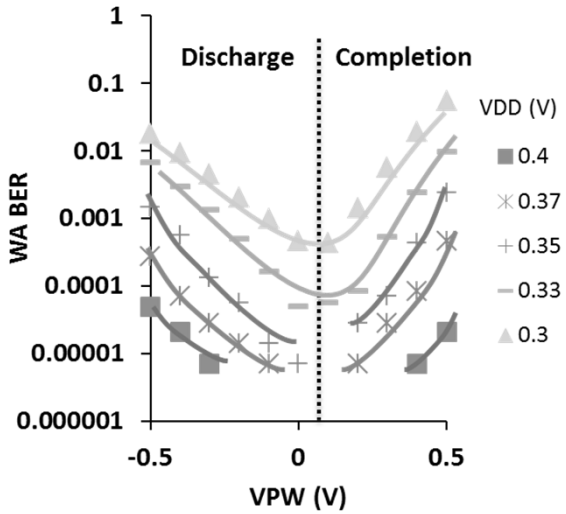
SRAM failure map



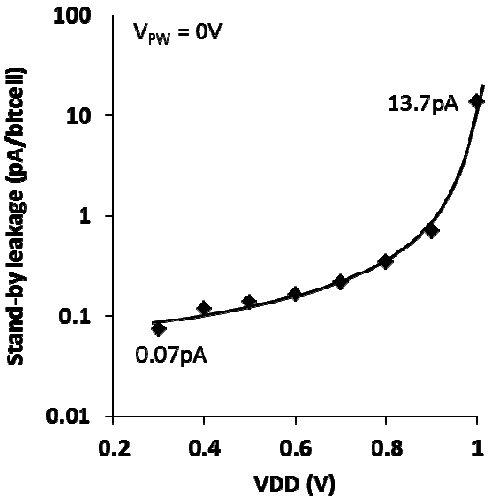
V_{MIN}



Failure mechanisms



Static consumption



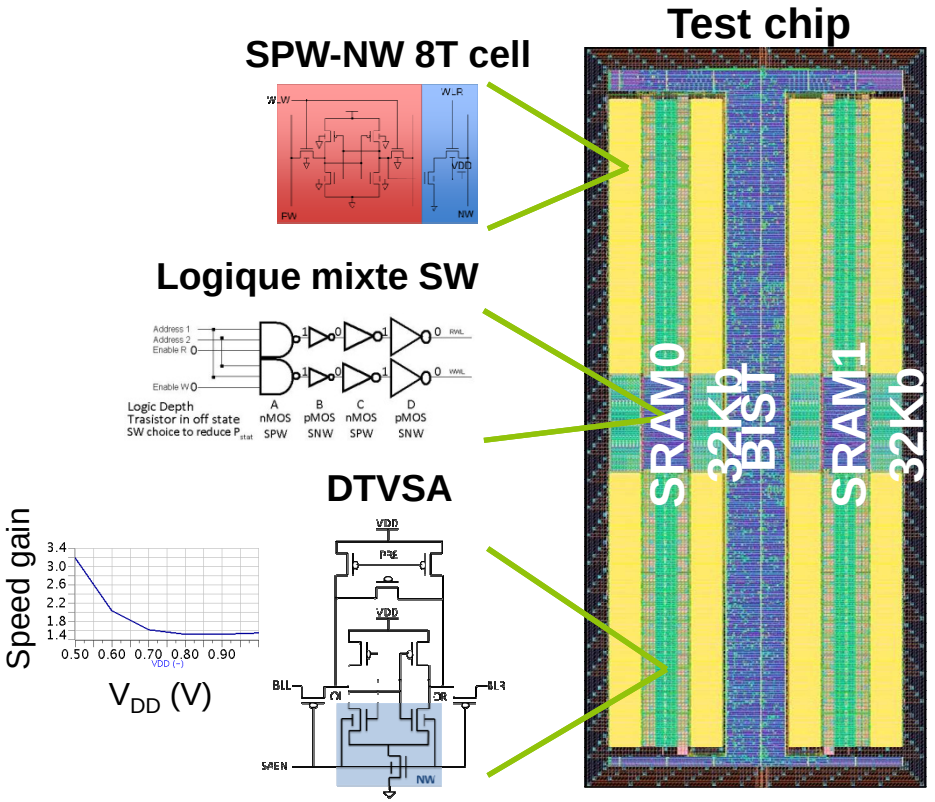
ESSDERC'14, IEDM'14

ULTRA-WIDE-VOLTAGE-RANGE MEMORY

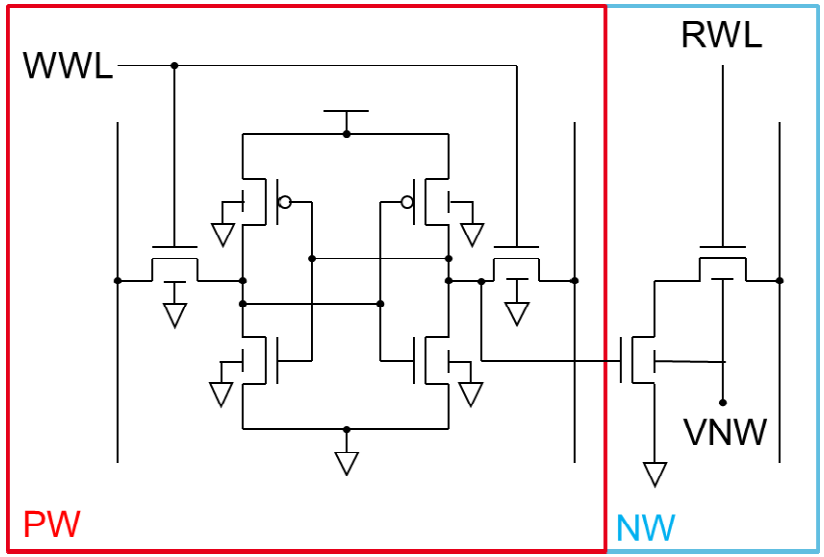
- Typically weak point in power management techniques

⇒Vidocq chip

- FDSOI 28nm
- Energy per access (32b) ~ **2pJ @1V** (Etat de l'art: 3pJ)
- Performance >1,5GHz @1V
- Vmin~ 400mV



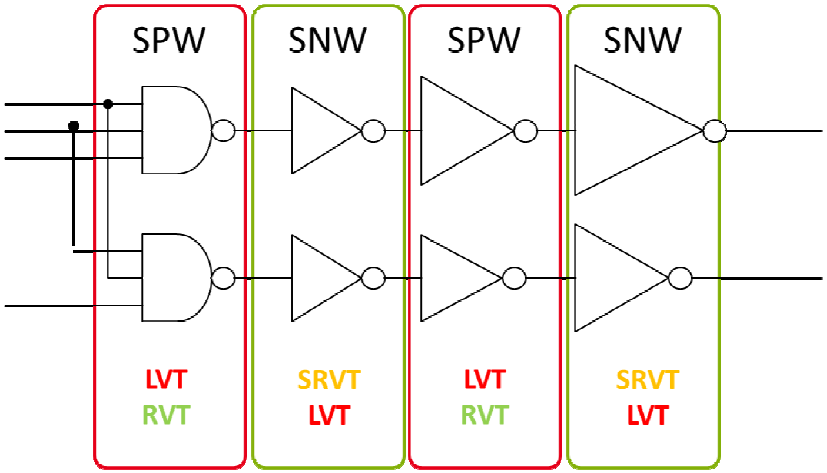
UWVR 32KB SRAM CUT



SPW 6T core *SNW read port*

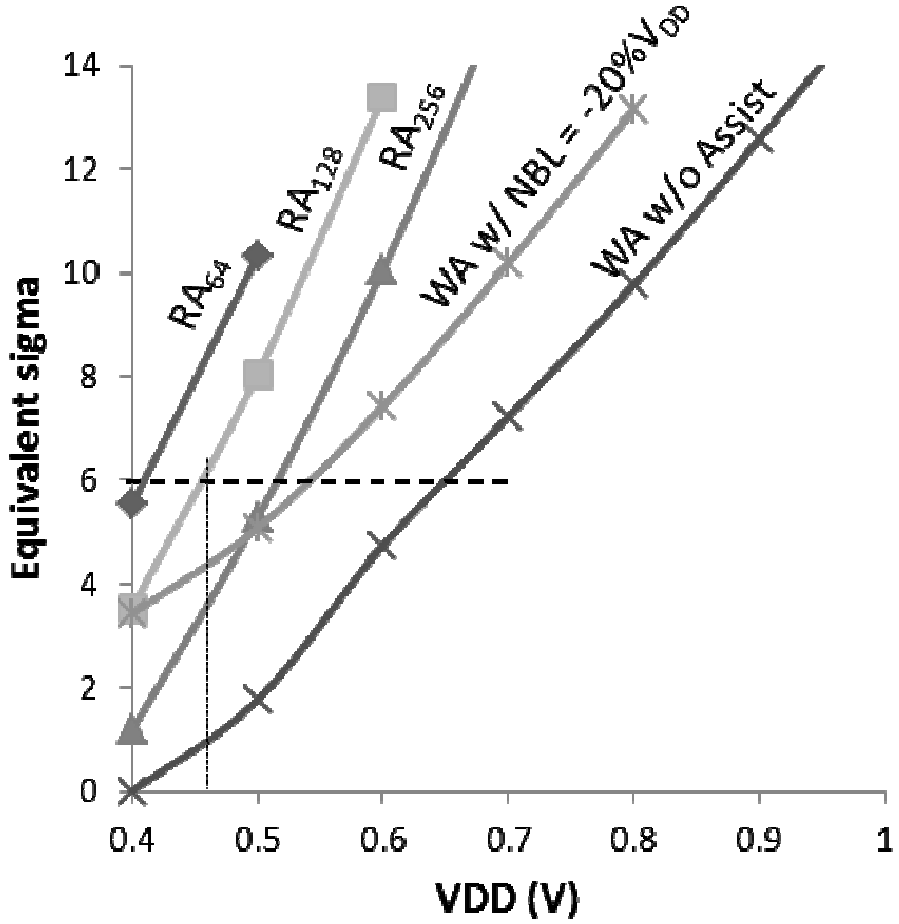
SPW-NW 8T bit-cell

Mixed-SW Row Decoder



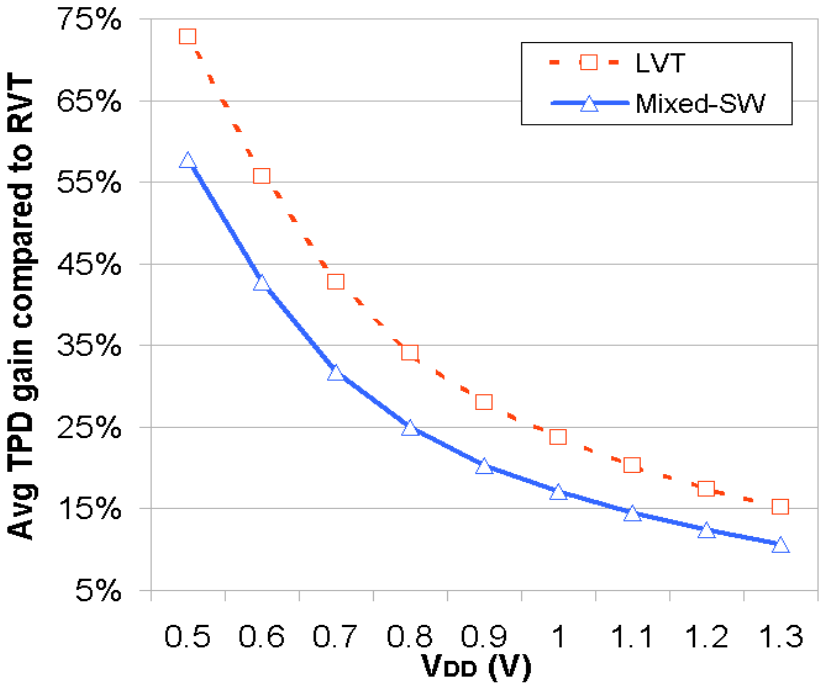
SOI-Conference'13, SOI-Conference'14, DAC'14

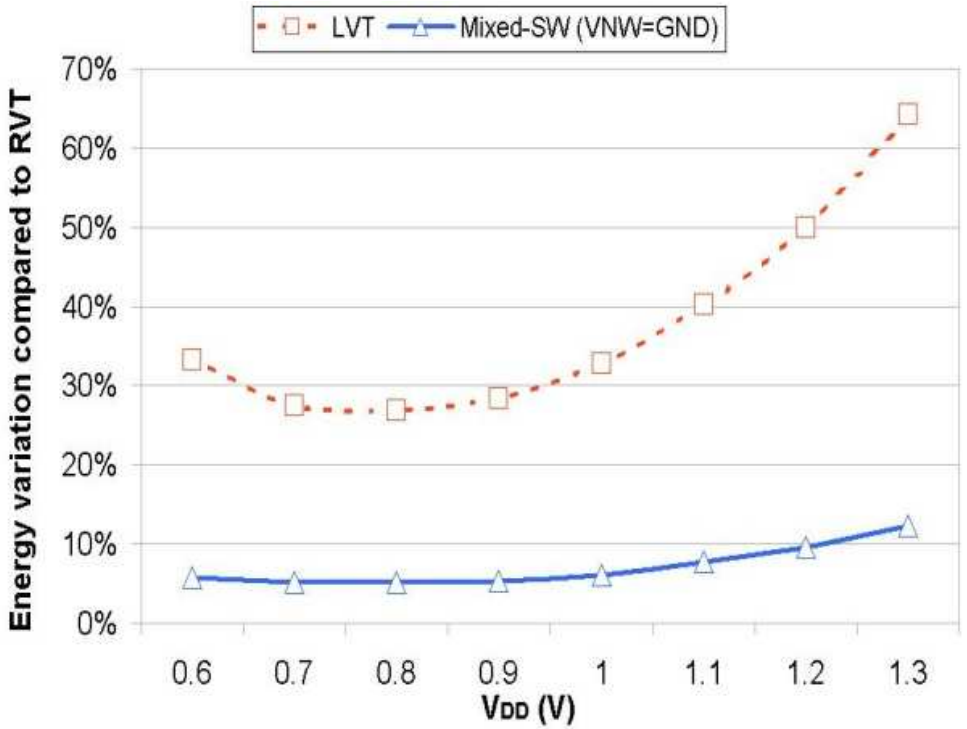
UWVR 32KB SRAM CUT: IMPROVED VARIABILITY



SOI-Conference'13, SOI-Conference'14, DAC'14

UWVR 32KB SRAM CUT: RESULTS





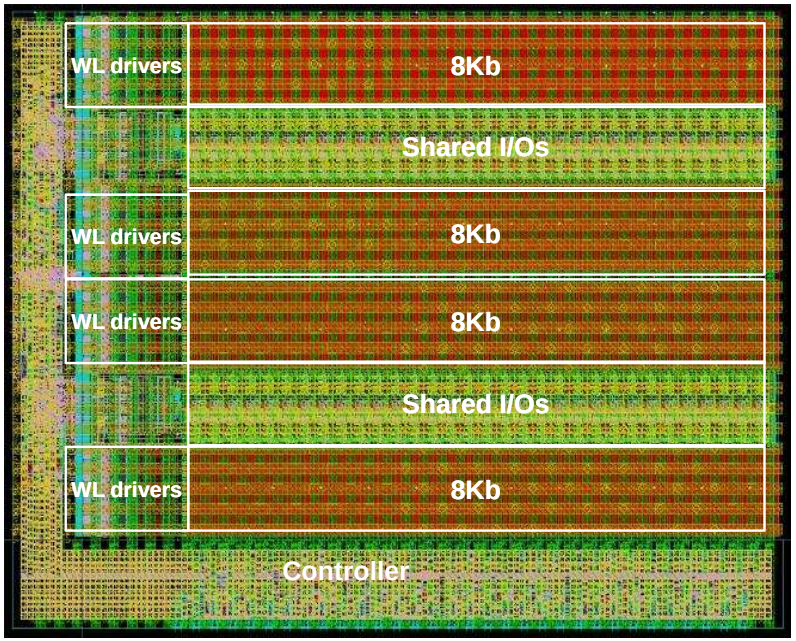
SOI-Conference'13, SOI-Conference'14, DAC'14

OUTLINE

- **FDSOI technology overview**
  - From bulk to UTBB-FDSOI
  - FDSOI technology flavors
  - Comparison between the different options
- **UWVR & ULV applications**
  - FRISBEE UWVR test chip & design techniques
  - UWVR memory
  - ULV memory
  - ULV design gain

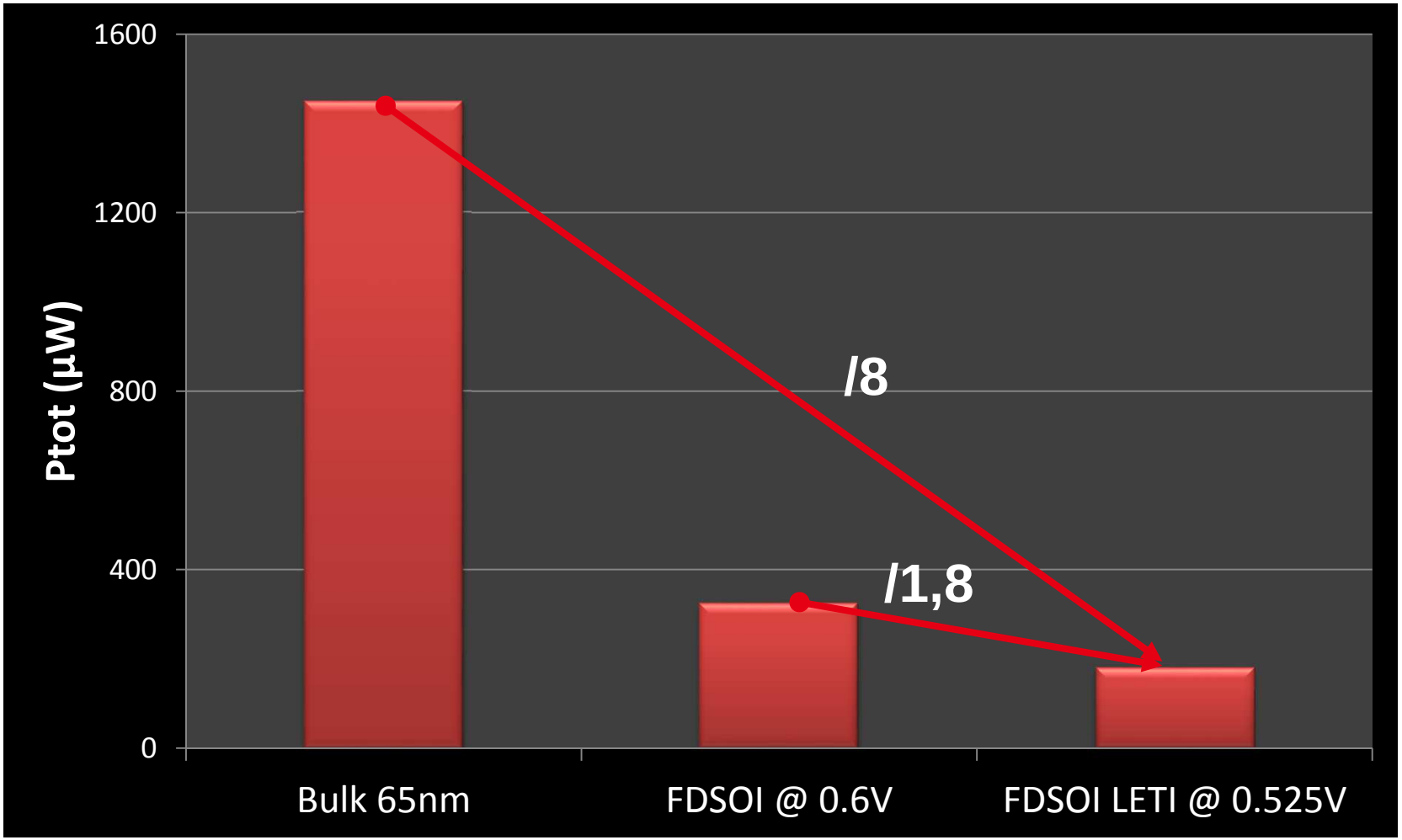
ULTRA-LOW-VOLTAGE MEMORY DESIGN

- **Constraints:**
  - Vdd = 0,5V
  - Fmax = 32 Mhz
- **Optimizations:**
  - Single-Pwell memory matrix
  - Single-Nwell periphery
  - Hierarchical power-gating of buffers
  - Multi Poly-Bias optimization
- **Results**
  - Area = 0,02 mm^2
  - Pleak = 1,97 µW @ ff 55°C
  - Pdyn = 1,37 µW/MHz @ ff 55°C



ULV DESIGN: FDSOI BOOST

- DSP + SRAM @ Iso-Performance (32 MHz)



SUMMARY

- **FDSOI allows Ultra-Wide-Voltage-Range thanks to dynamic VT control**
- **Burst modes COMBINED with high energy efficiency point is now affordable**
- **ULV design optimization can provide up to 80% gains wrt bulk**

⇒ LETI added value is to share his knowledge and methodology, to provide the IPs and the control algorithms for statically and dynamically managing the performance / energy efficiency / low leakage tradeoffs

Q/A

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