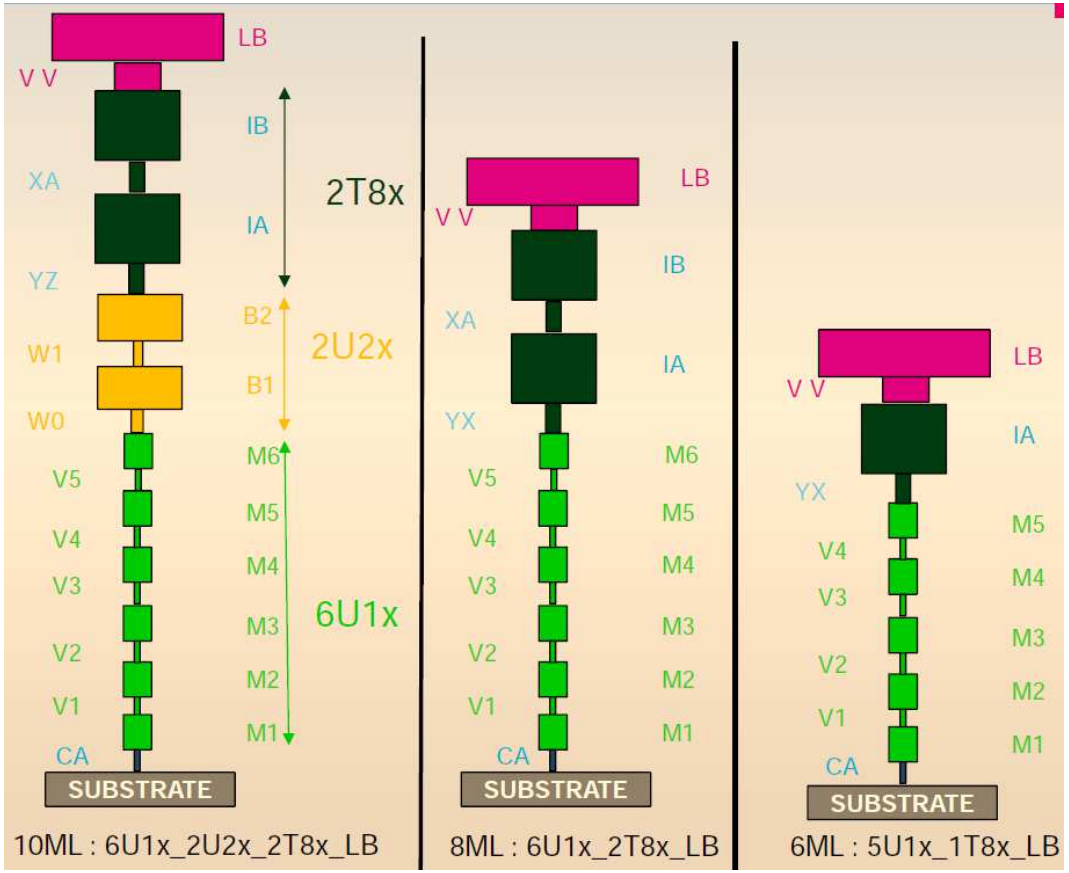
FD-SOI FOR RF IC DESIGN

SITRI – LETI Workshop | Mercier Eric | 08 september 2016

UTBB 28 nm FD-SOI : RF DIRECT BENEFITS (1/2)

- **3 back-end options available**



- Routing possible on the AluCap level ➔ no restriction vs. 0.7 % in 65 nm

UTBB 28 nm FD-SOI : RF DIRECT BENEFITS (2/2)

- **Capacitors**

Capacitor	Density (Typical)	Observation
egncap	10.1fF / µm²	GO2 device (thick gate oxide)
CMOM - M1 to M5 (max)	6.45fF / µm²	Space(finger) = Width(finger) between 50 and 100nm Vmax = 1.1V for S=W < 80 nm Vmax = 1.8V for S=W > 80 nm
CMIM	16.2fF / µm²	process option : add 3 masks Total area max = 24.6mm² Vmax = 1.155V
lvtnfet (Vg =1V … Vx =0V)	~18fF / µm²	Used as loop filter or supply bypass capacitor Depends on the config. Low capacitance for low voltage.
lvtpfet (Vb =1V … Vx =0V)	~17fF / µm²	Used as loop filter or supply bypass capacitor Depends on the config. Low capacitance for low voltage.

- Very good density / less parasitics to substrate
- Interesting MIM capacitor quality factor

- All required devices for RF exist in FD-SOI

UTBB-FDSOI 28nm FOR ULP RF (1/4)

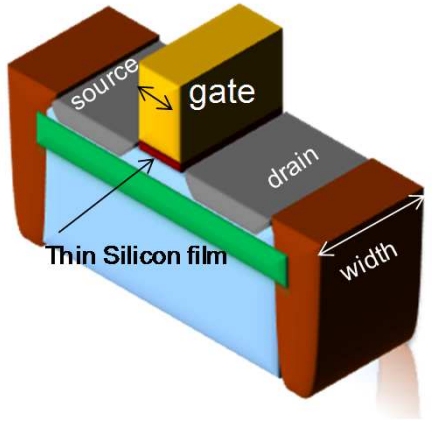
ACTIVE DEVICES PERFORMANCE AND COMPARISON

- **No channel doping : better gain compare to bulk**
  - At 0.18 µm gate length, the analog gain Gm/Gd in weak inversion in FD-SOI 28nm is higher than the 180 nm CMOS

	0.18CMOS	28nmBulk	FDSOI28nm
Gm/Gd	50	25	75

  - At 1 µm gate length, the Gm/Gd on FDSOI is 6 time larger than the CMOS 28 nm bulk

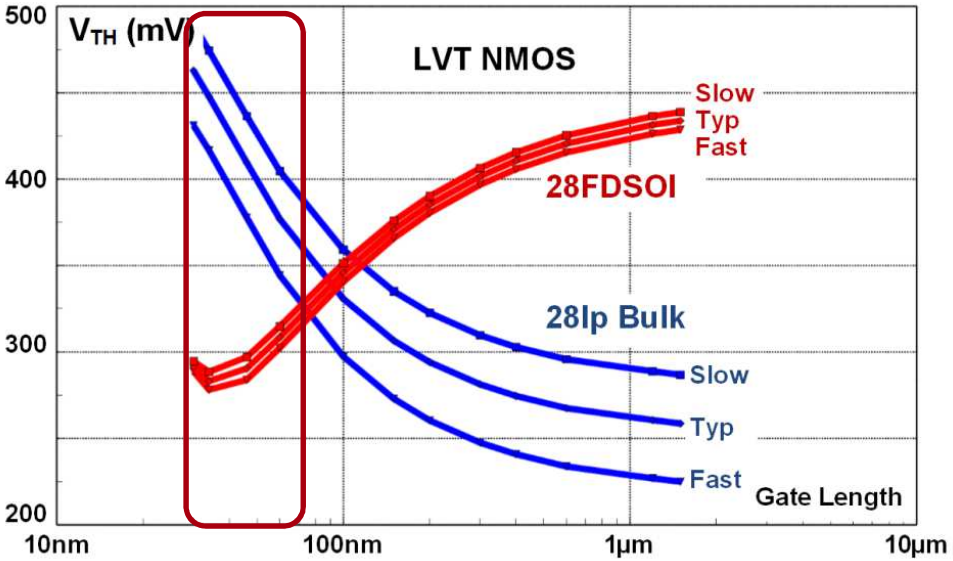
	28nmBulk	FDSOI28nm
Gm/Gd	50	300



UTBB-FDSOI 28nm FOR ULP RF (2/4)

HIGH SPEED ANALOG PERFORMANCE

- **Lower Vth, less variability**
  - Design at Low Power supply
  - High dynamic range
    - With respect to V_{DD} versus V_{th}
  - Analog compatible minimum gate lengths



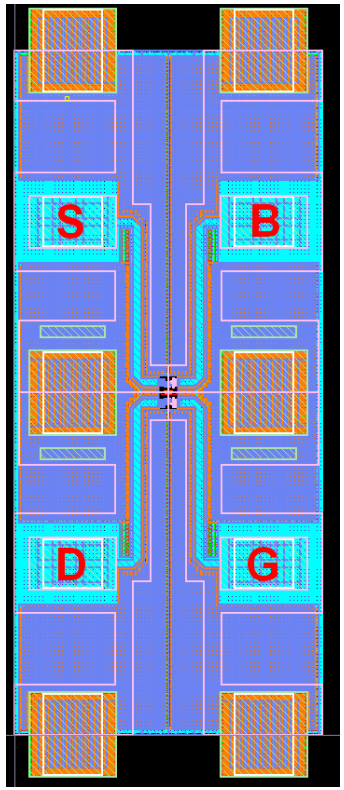
- **Reduced S/D capacitances**
  - Increased comparator BW
  - Faster logic
  - Reduced switch parasitic
  - Less Power comsumption

UTBB-FDSOI 28nm FOR ULP RF (3/4)

HIGH RF PERFORMANCES ON BOTH FRONT- & BACK-GATE

- **Front Gate FT : faster transistor even at low power supply**
  - FT: 300 GHz @ 1 volts V_{DD}
  - FT: 150 GHz @ 0.3 Volts V_{DD}

MEASUREMENTS DONE at LETI



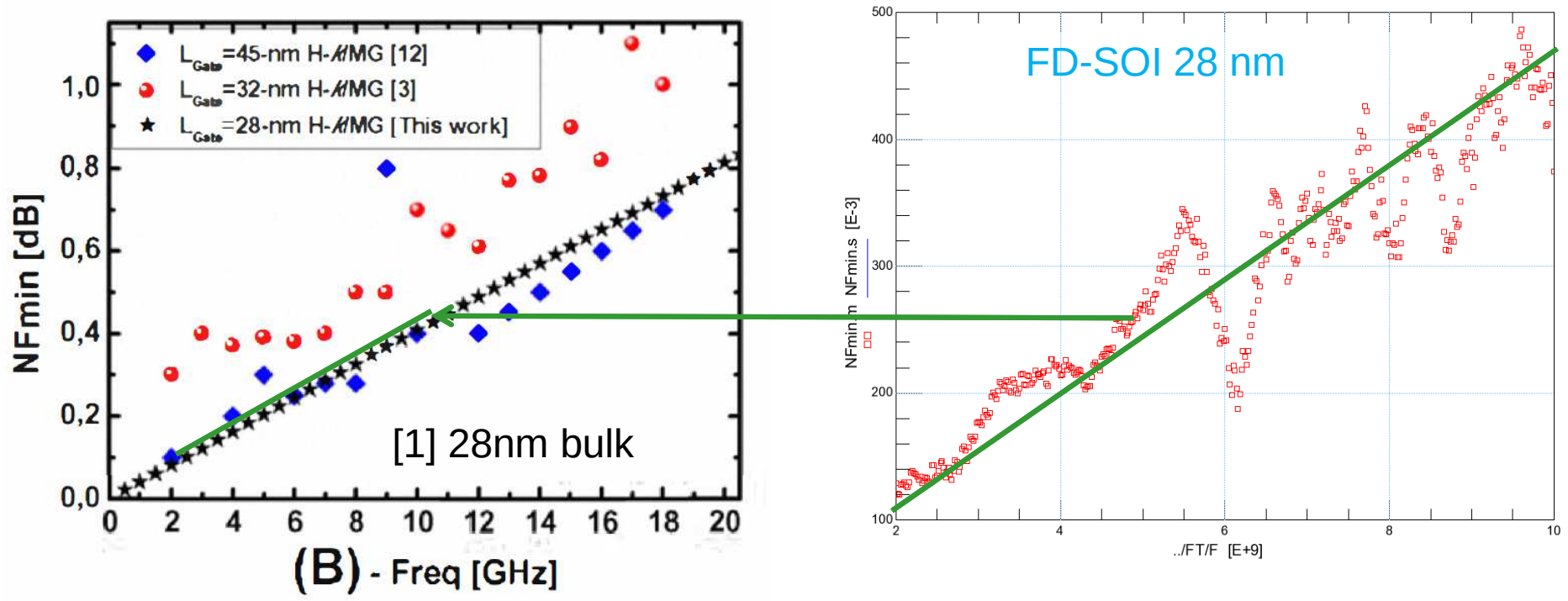
- **Back gate useful for RF ➔ simple design**
  - FT: 80 GHz @ 1 volts V_{DD}
  - FT: 40 GHz @ 0.3 volts V_{DD}

UTBB-FDSOI 28nm FOR ULP RF (4/4)

LOW NOISE PERFORMANCE

- NF_{min} ≈ 0.2dB (F = 2 GHz), ≈ 0.4dB (F = 10 GHz)
- Noise performances similar to 28nm Bulk

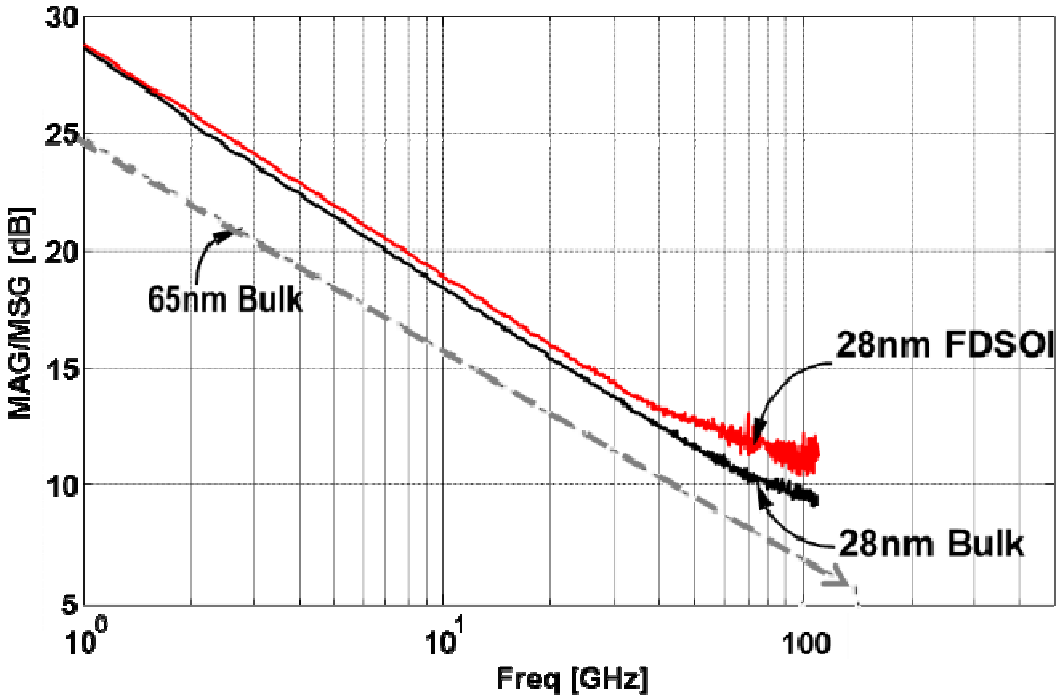
Ids=135 mA/mm, Lg=30nm



[1] Y. Tagro et al "RF Noise Investigation in High-k/Metal Gate 28-nm CMOS Transistors" IEEE IMS, june 2012

UTBB-FDSOI 28nm : FROM RF TO mmW

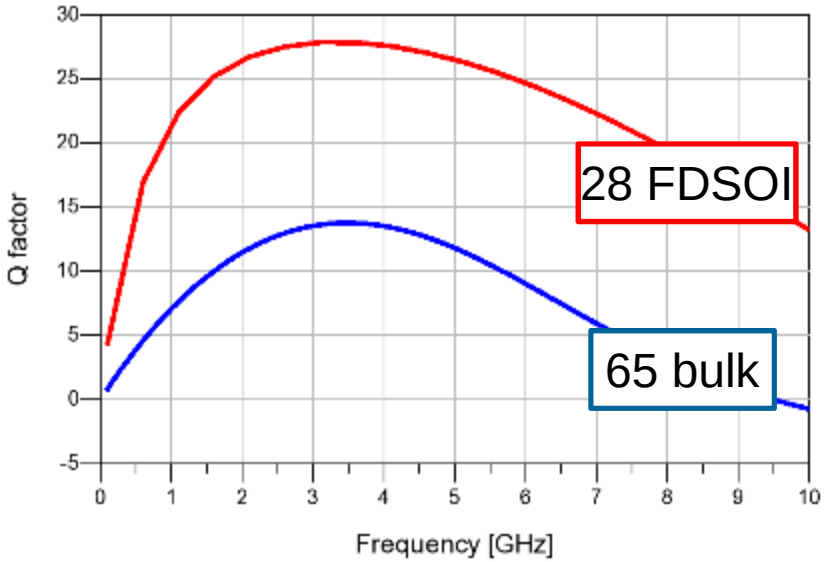
- **Active devices performance and comparison (RF)**
  - Higher Gain than CMOS 28 nm & 65nm technology

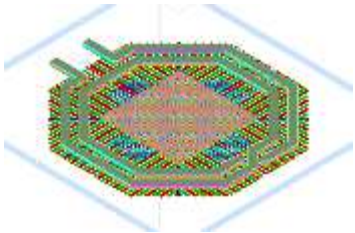


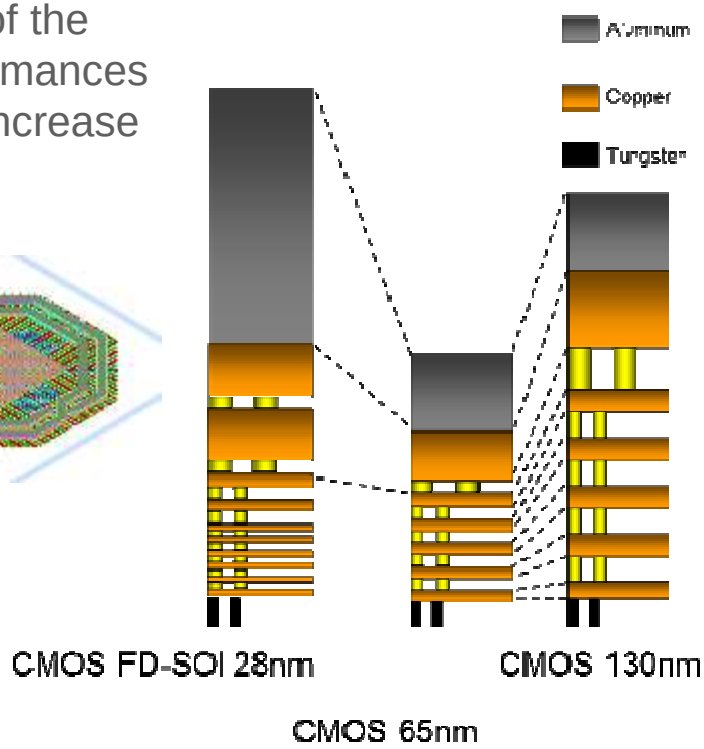
4 dB gain improvement with respect to CMOS 65nm at 2.4GHz

UTBB-FDSOI 28 nm FOR ULTRA LOW POWER RF

- **Passive devices performance**
  - Typically, the CMOS trend to vertically shrink of the Back-End Of Line (BEOL) penalizes RF performances
  - The small metal pitch and the thin dielectrics increase the Resistance/Capacitance ratio



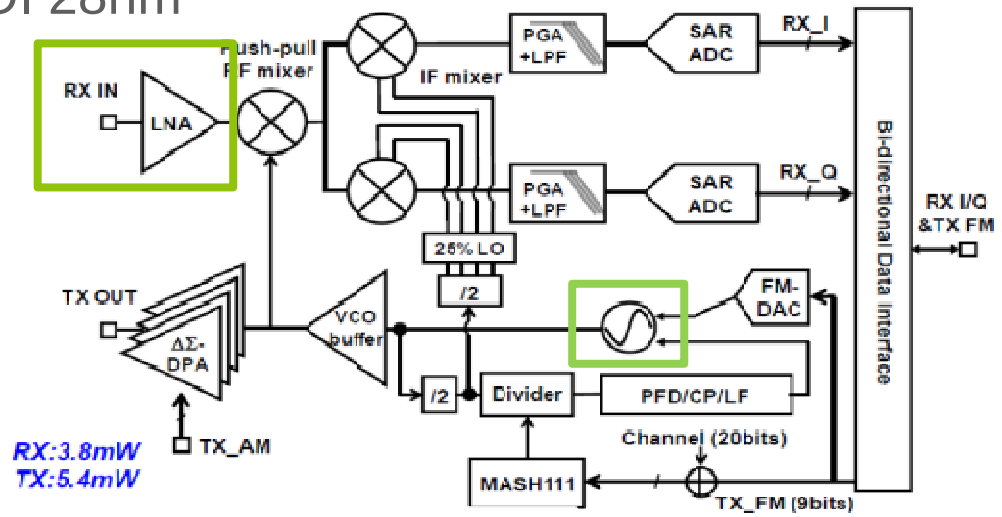




1.5nH inductor offers 25 Q factor value in UTBB-FDSOI 28nm

CMOS 65 nm vs FDSOI 28nm : RF BENCHMARK

- **Comparison between two usual RF blocs**
  - LNA and VCO
- **Technology use :**
  - CMOS 65 nm : 7metal layers from STMicroelectronics
  - UTBB-FDSOI 28 nm : 10 metal layers from STMicroelectronics
- **Transistor models**
  - PSP or BSIM for CMOS 65nm
  - UTSOI 2 for UTBB-FDSOI 28nm

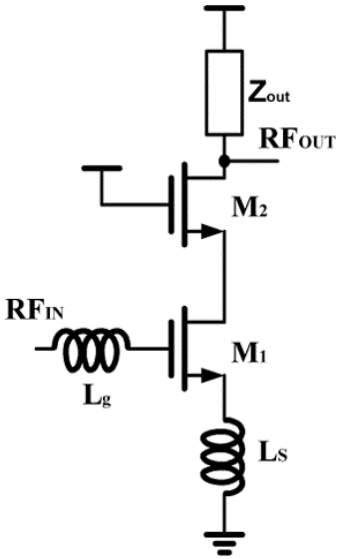


90nm BLE/15.4/15.6 Transceiver

[Y.H. Liu, ISSCC2013]

CMOS 65 nm vs FDSOI 28nm : RF BENCHMARK

LOW NOISE AMPLIFIER : 2.4GHZ TEST CIRCUIT



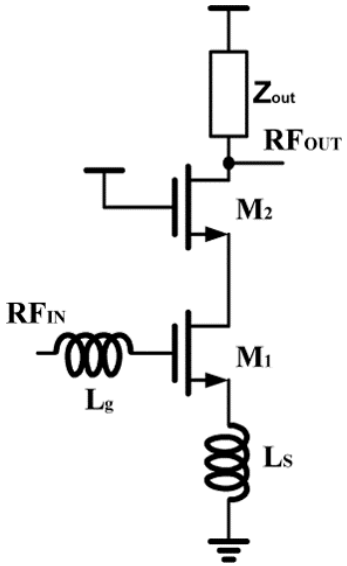
- Degenerated cascade topology
- Ls and Lg inductance used to match noise and input impedance (target <-10dB S11)
- Gain is evaluated considering Zout = LNA conjugate output impedance
- Same inductor Q value (ideal component with set Q factor)

LETI BENCHMARK 2015

	CMOS 65nm	UTBB-FDSOI 28nm
NMOS Family	N-lvt	N-lvt
Inductance Q value	10	10
Nominal Vdd (V)	1.2	1

CMOS 65 nm vs FDSOI 28nm : RF BENCHMARK

LOW NOISE AMPLIFIER : 1 mW SCENARIO



LETI BENCHMARK 2015

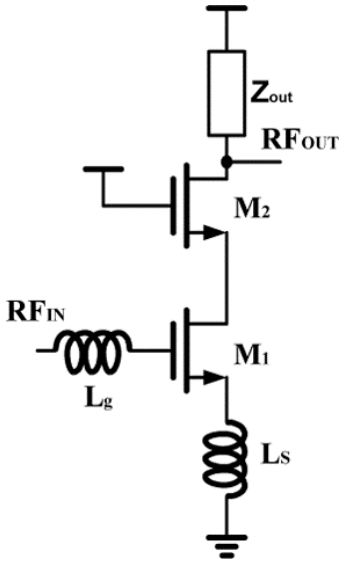
FoM	CMOS 65nm	UTBB-FDSOI 28nm
NFmin (dB)	0.9	0.9
Gain* (dB)	21	25
S11 (dB)	-11	-16
P_{DC} (mW)	1	1
IIP3 (dBm)	-15	-15
ICP1 (dBm)	-24	-24

**Power Gain considering a perfect match output*

4dB gain improvement in FD-SOI for same power

CMOS 65 nm vs FDSOI 28nm : RF BENCHMARK

LOW NOISE AMPLIFIER : ULTRA LOW-POWER SCENARIO



LETI BENCHMARK 2015

FoM	CMOS 65nm	UTBB-FDSOI 28nm
NFmin (dB)	1	1
Gain (dB)	21	24
S11 (dB)	-10	-10
P_{DC} (mW)	0.4@1.2V	0.1@0.55V*
IIP3 (dBm)	-30	-26
ICP1 (dBm)	-39	-36

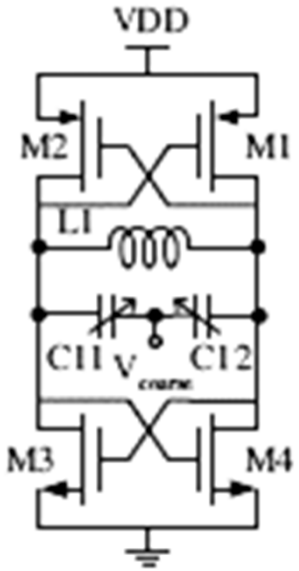
**Using body bias = 350mV*

X4 power consumption decrease with same RF performances

CMOS 65 nm vs FDSOI 28nm : RF BENCHMARK

TEST CIRCUIT : 2.4GHz

- **VCO**



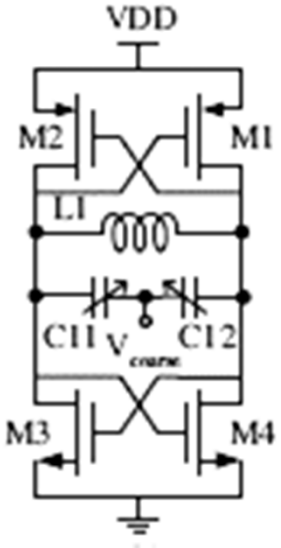
LETI BENCHMARK 2015

- CMOS cross-coupled topology
- Same inductor Q value
  - Ideal component with set Q factor

	CMOS 65nm	UTBB-FDSOI 28nm
NMOS Family	N-lvt / P-lvt	N-lvt / P-lvt
Tank Q value	15	15
Nominal Vdd (V)	1.2	1

CMOS 65 nm vs FDSOI 28nm : RF BENCHMARK

VCO : 1 mW / 0.2 mW SCENARIO



FoM	CMOS 65nm	UTBB-FDSOI 28nm
Frequency (GHz)	2.4	2.4
Phase Noise (1MHz in dBc/Hz)	-119	-126
P_{DC} (mW)	1	1
Phase Noise (1MHz in dBc/Hz)	-105	-117
P_{DC} (mW)	0.2 @ 0.8V	0.2 @ 0.7V

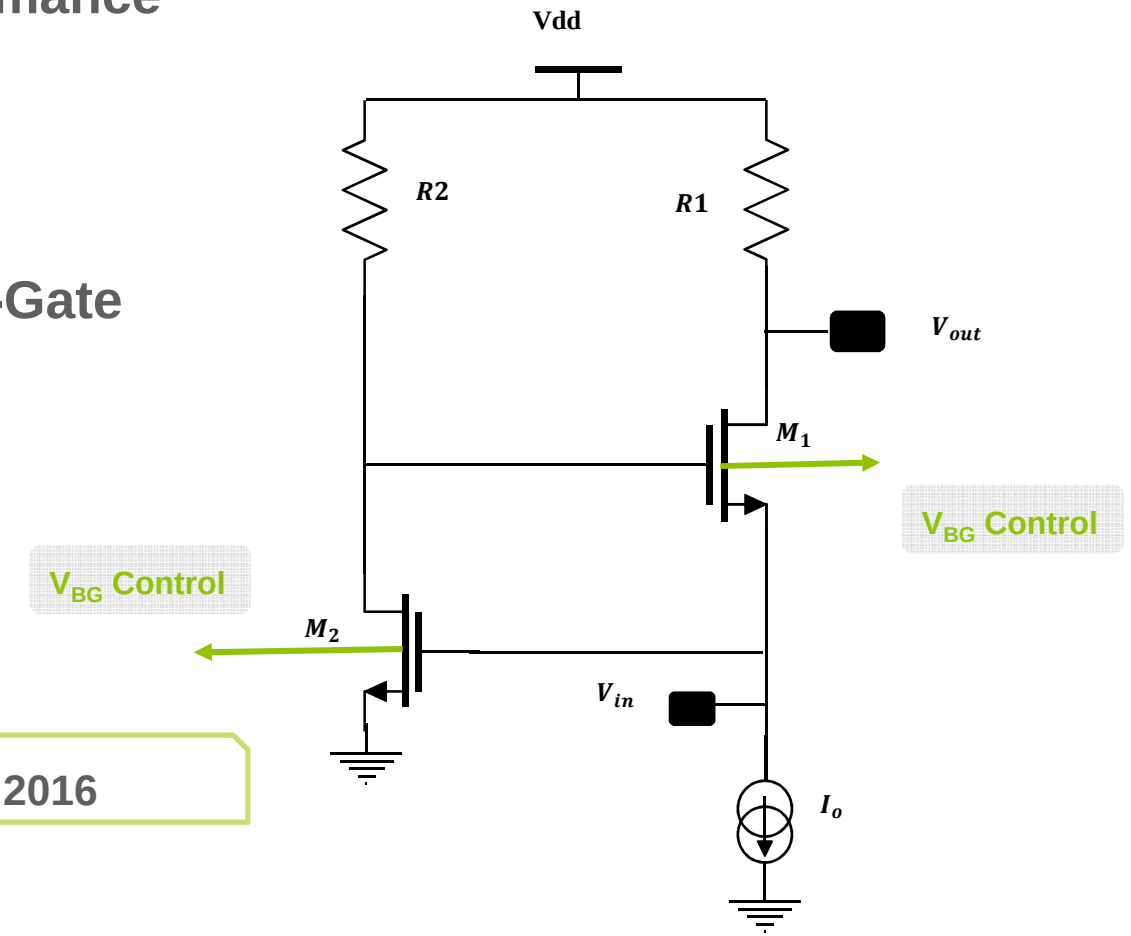
LETI BENCHMARK 2015

7 dB to 12 dB Phase Noise improvement for the same power consumption

SPECIFIC FDSOI BENEFITS FOR LNA

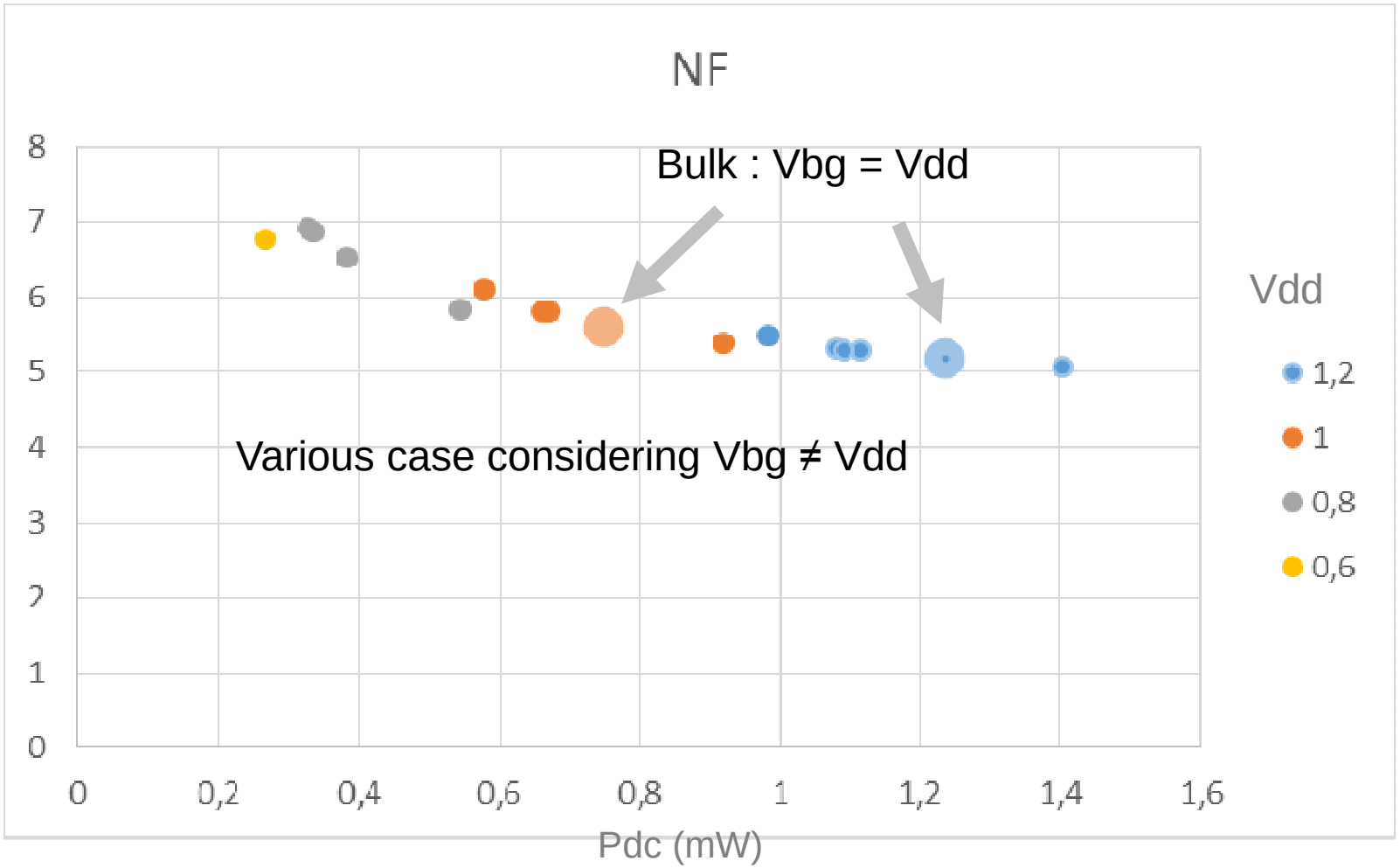
- **Evaluation of the performance**
  - For the Gain in V (dB)
  - For the NF (dB)

- **Making use of the Back-Gate**



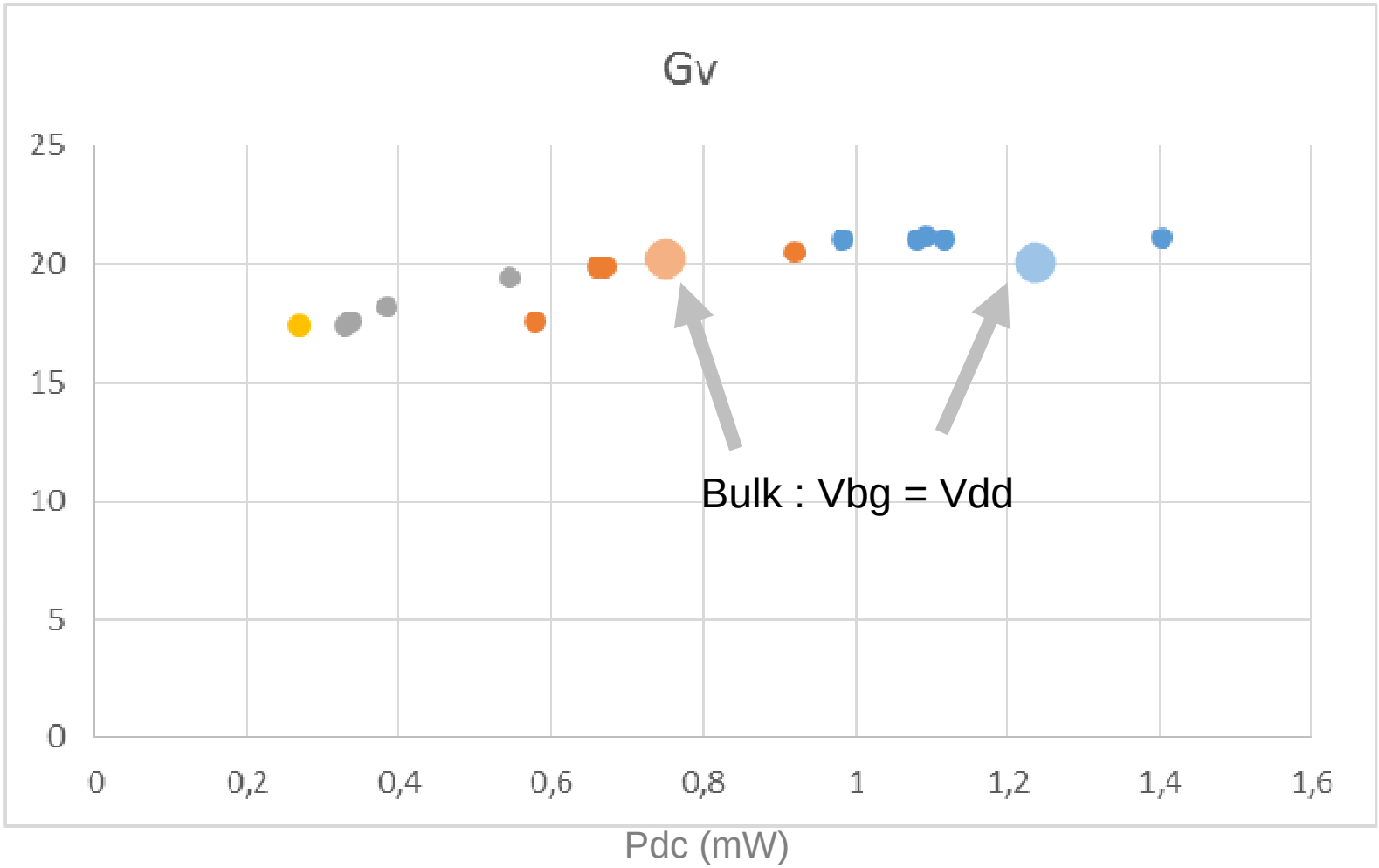
LETI EVALUATION 2015 / 2016

BACK-GATE CONTROL FOR LNA (1/3)



FDSOI : good candidate for ULV use

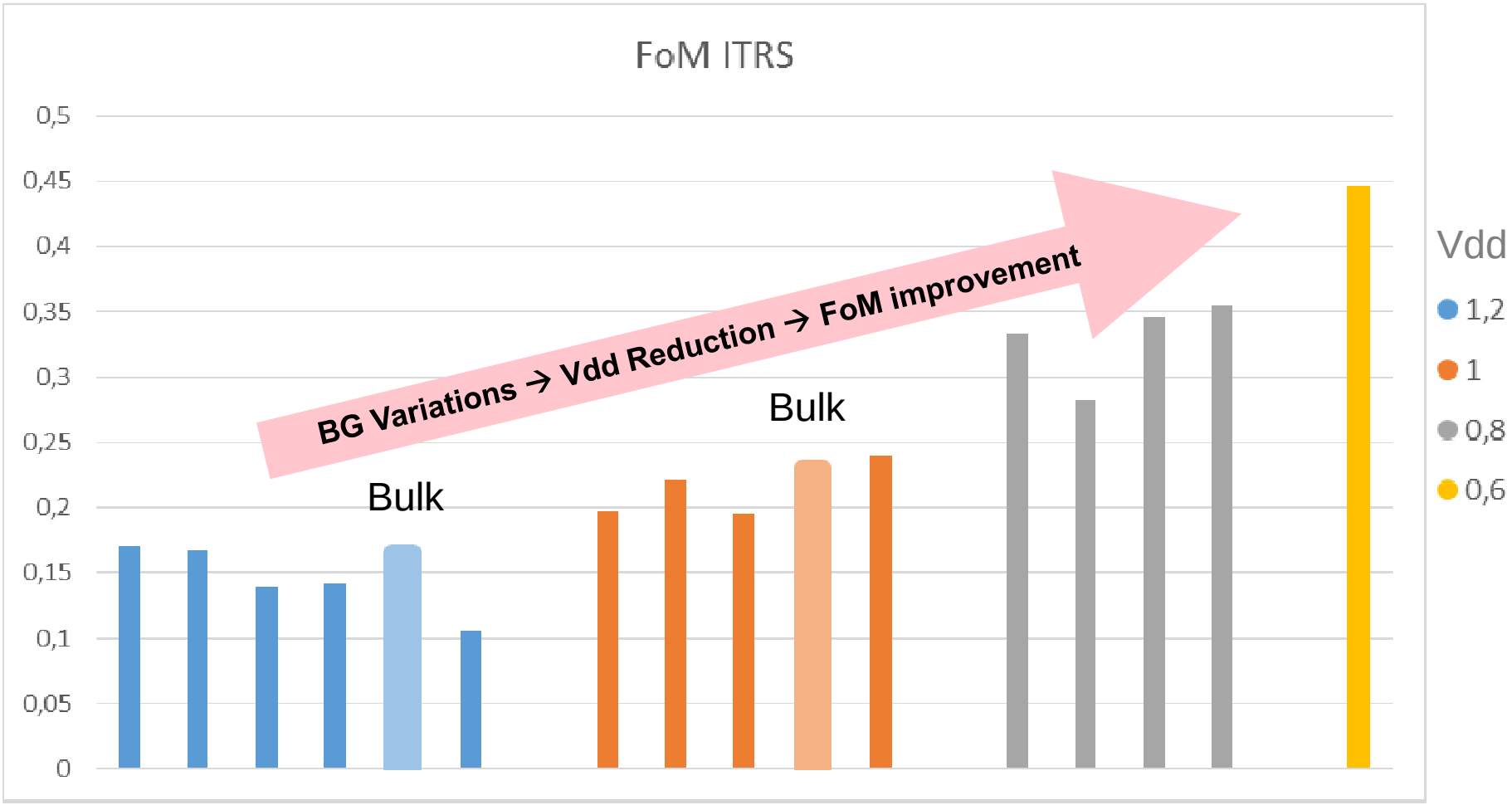
BACK-GATE CONTROL FOR LNA (2/3)



FDSOI : good candidate for reconfigurability

BACK-GATE CONTROL FOR LNA (3/3)

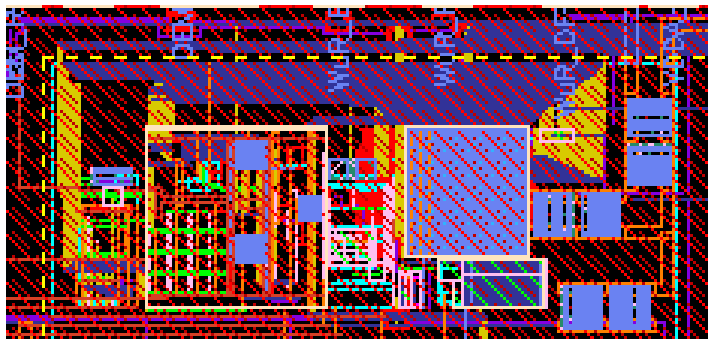
$$FOM = \frac{Av.freq.IIP3}{(Fmin-1)(Id.Vdd)}$$



ULP RF – ALWAYS ON / WAKE-UP REALIZATION

LETI FULL FRONT-END 2016

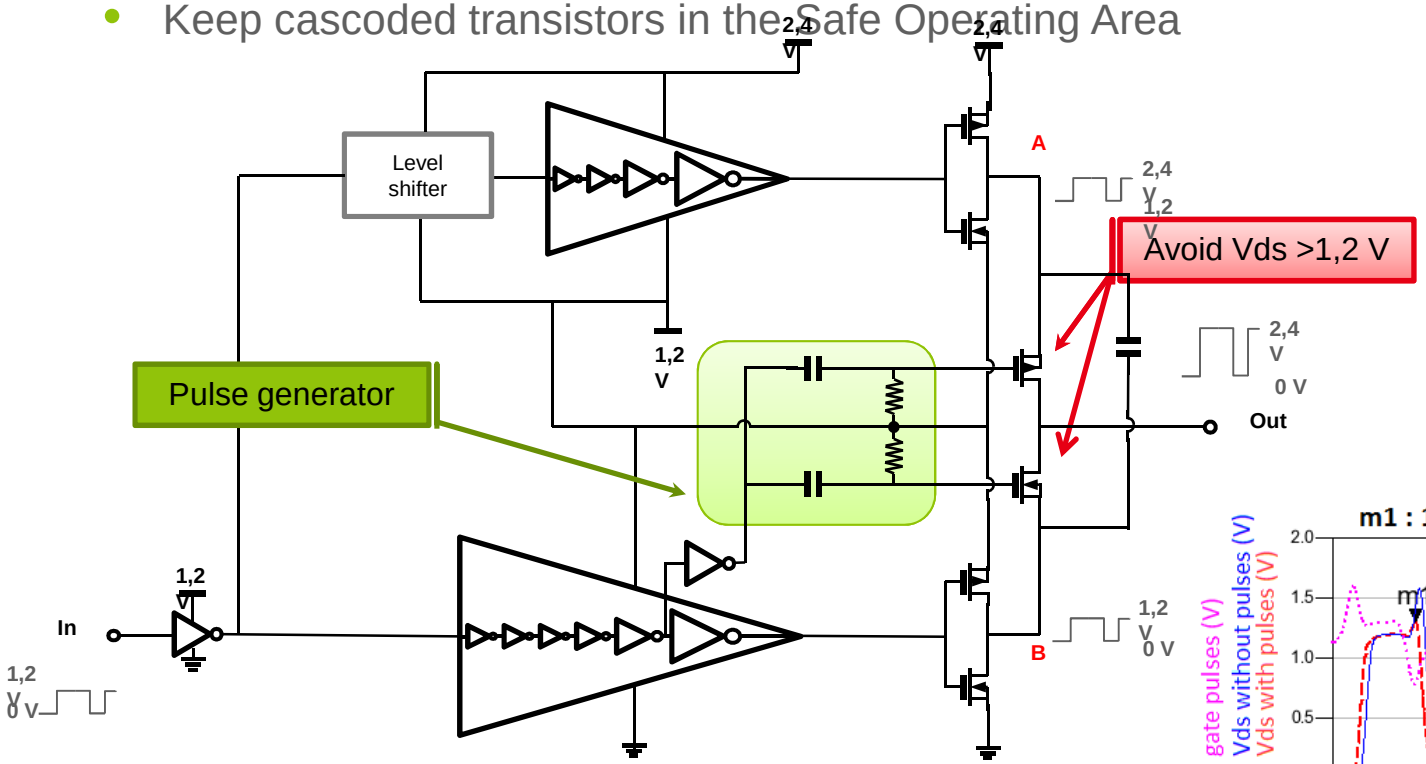
- **Multi band capability**
  - 868-915 MHz / 1.4 GHz / 2.4 GHz
  - Highly Flexible : Carrier Frequency, Modulation, Channel condition, etc…
  - No costly external component
  - Improved Robustness
- **Adaptive power consumption**
  - Event-driven activity
  - Target to burn **~ 50 µW in active mode**
  - Analog front-end to demodulation : 20 µW
  - Synthesizer and LO : 30 µW
- **Fast power-on time**
- **Low-cost and easy implementation**
  - Inductorless design
  - Calibrationless design
  - FD-SOI 28 nm

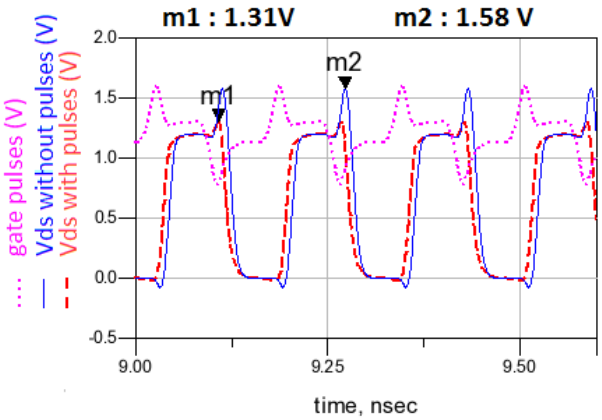


Snapshot of the full Wake-Up RX

HIGH-SPEED MODULATOR DRIVER - BULK

- **CMOS bulk**
  - Additionnal circuitry required
  - Keep cascoded transistors in the Safe Operating Area

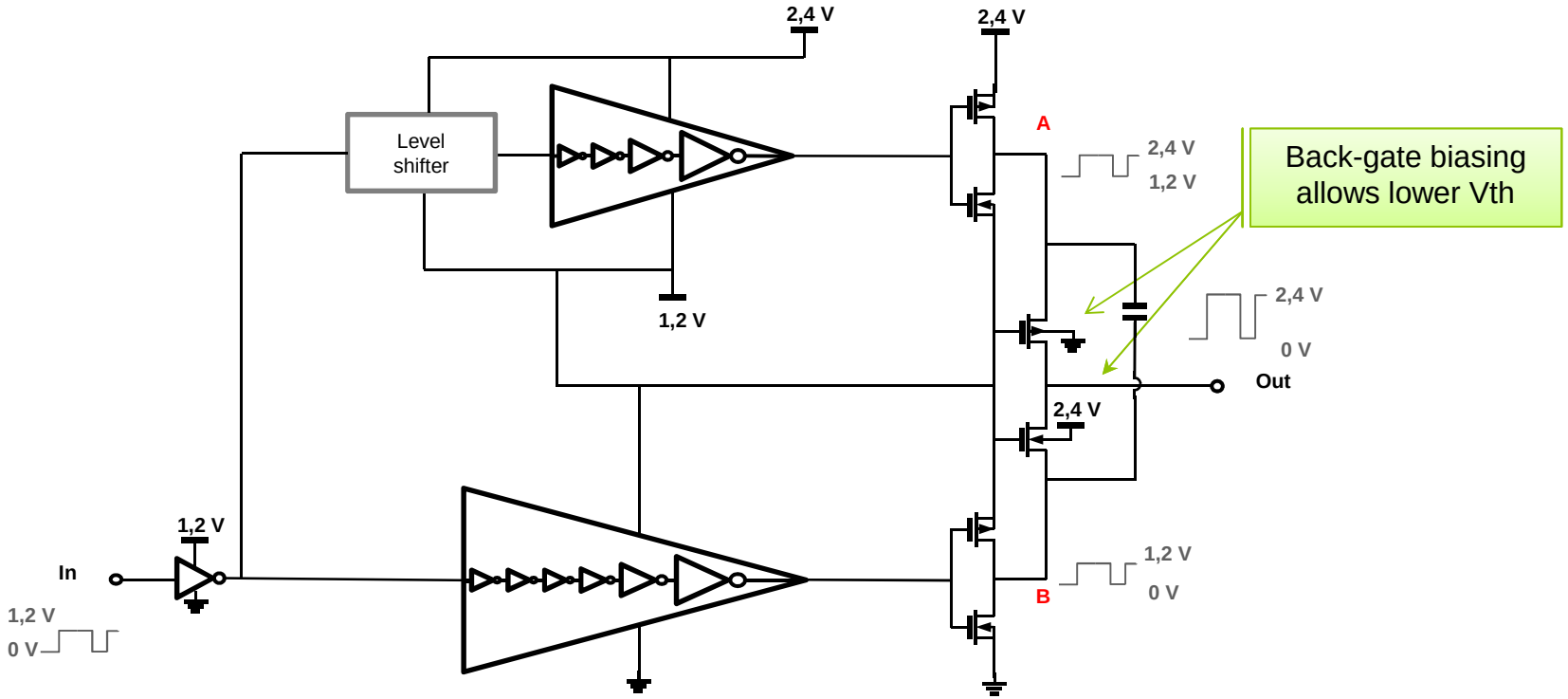




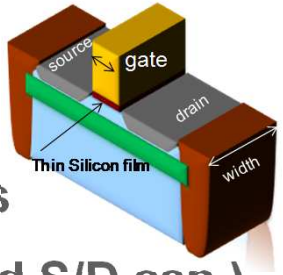
HIGH-SPEED MODULATOR DRIVER - FDSOI

LETI FULL TX/RX 2016

- **FDSOI 28 nm**
  - Back-Gate allows Vth reduction ➔ no Vds over-voltage
  - Very High Speed communications : 25 Gbps

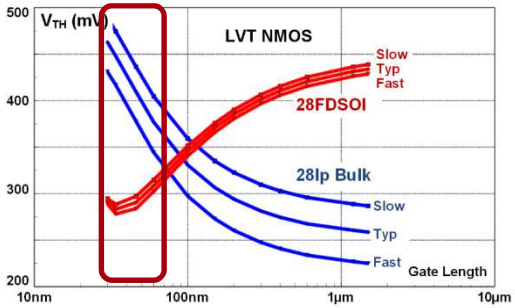


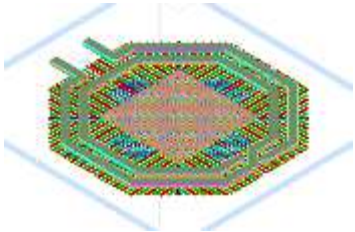
WIRELESS COMMUNICATION : FD-SOI VS BULK



- Gain improvement (no channel doping)
- Higher speed / analog performance / reduced parasitics
- Higher Passive Quality factors (Metal options & reduced S/D cap.)
- Lower power and higher dynamic range / Lower V_{TH}
- Higher frequency operation / faster transistors for lower power
- Easier design / Back Gate as a Static & Dynamic

1µm Length	28nmBulk	FDSOI28nm
Gm/Gd	50	300





BETTER GAIN | BETTER PHASE NOISE | ULTRA LOW POWER

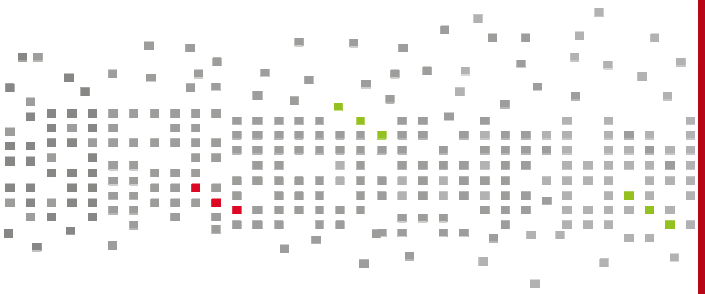
FD-SOI RF DESIGN

CURRENT OFFER FROM LETI in FD-SOI

- **ULP RF Front-End : TX and RX**
  - Multi-Standard / Multi-Mode (2016 / 2017)
- **ULP Always-On RX Front-End**
  - Wake-up function / spectrum sensing (2015 / 2016)
- **Very High Speed Optical Driver / Modulator / Receiver**
  - Increase speed rate to tackle the 56 Gbps (2016)
- **Fast & High-Resolution ADC : 100 MSpsp / 12 bits**
  - General purpose / Low Power for RF Front-End (2016 / 2017)

ULP RF for IoT	Very High Speed OPTICAL DRIVER/RECEIVER	High Sampling Rate ADC

FD-SOI RF DESIGN



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