Integrated Circuits for Neural Implants

应用于植入式神经器件的集成电路

More than Moore · More than Innovation

Dr. Lei Yao 姚镭 博士

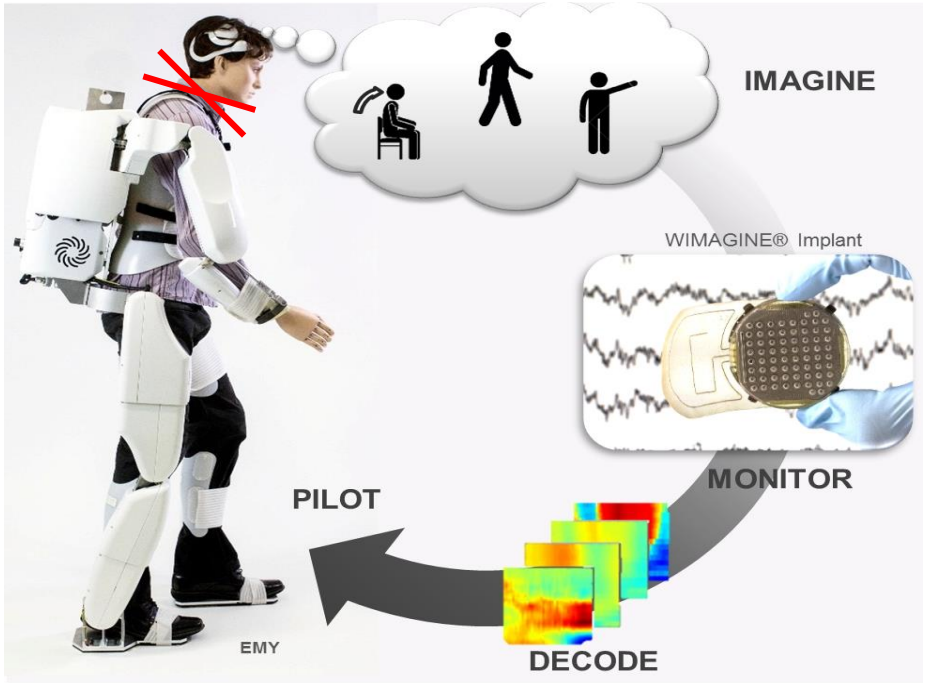
Director of Analog & Mixed Signal IC, SITRI

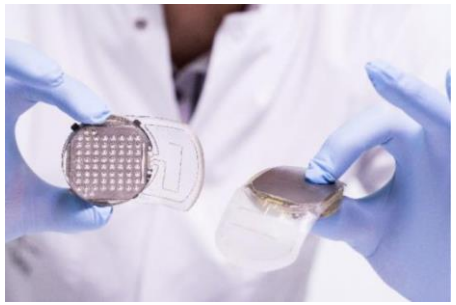
工研院模拟和混合信号IC部门总监

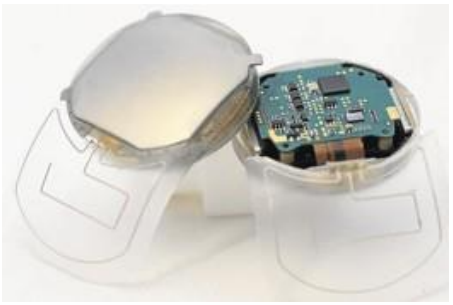
Nov. 13, 2019

Neural Implant
植入式神经器件

Source: www.cctv.com







Source: www.leti-cea.com

Neural Implant
植入式神经器件

Retinal implant
FDA 2013

Cochlear implant
FDA 1985

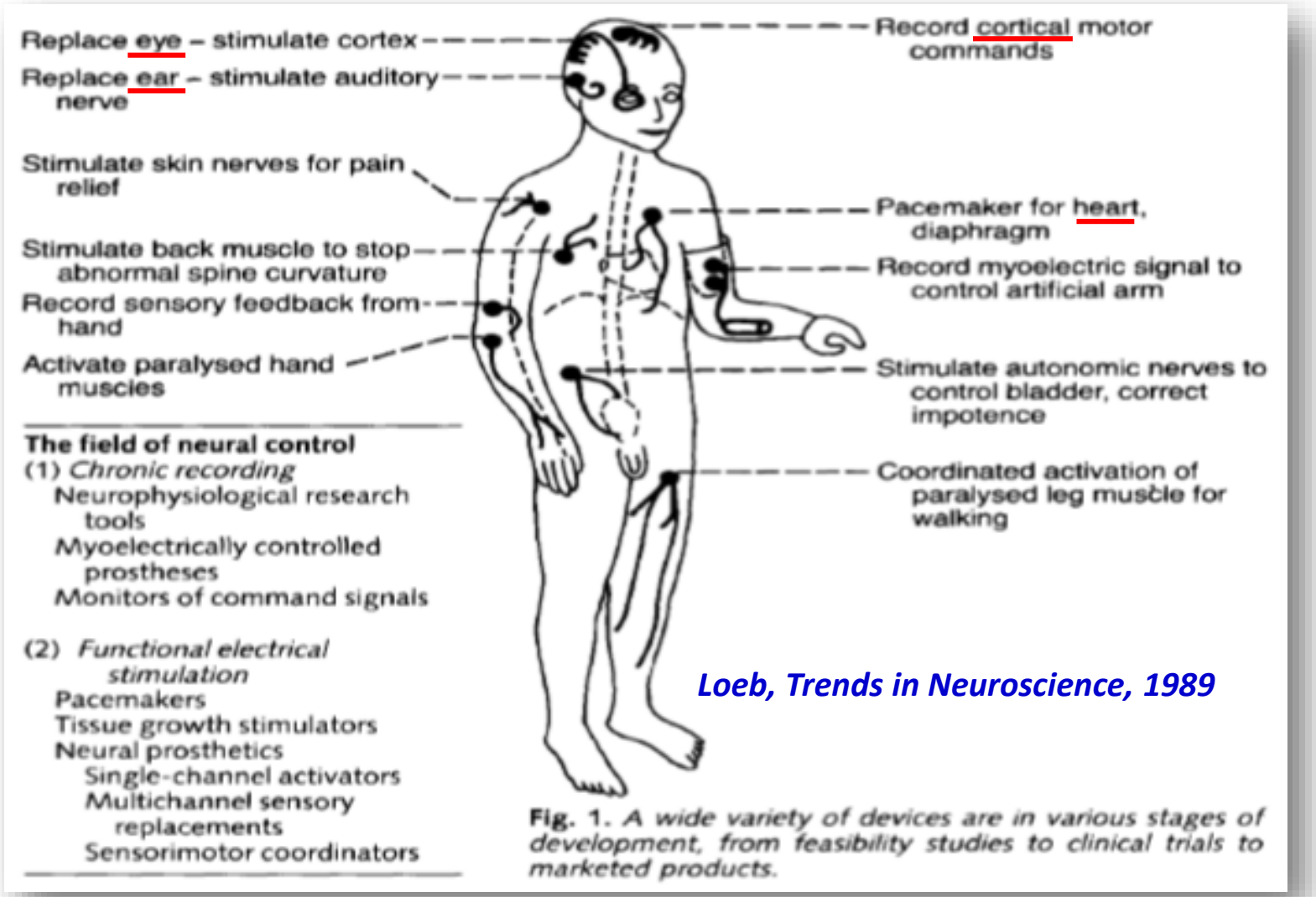


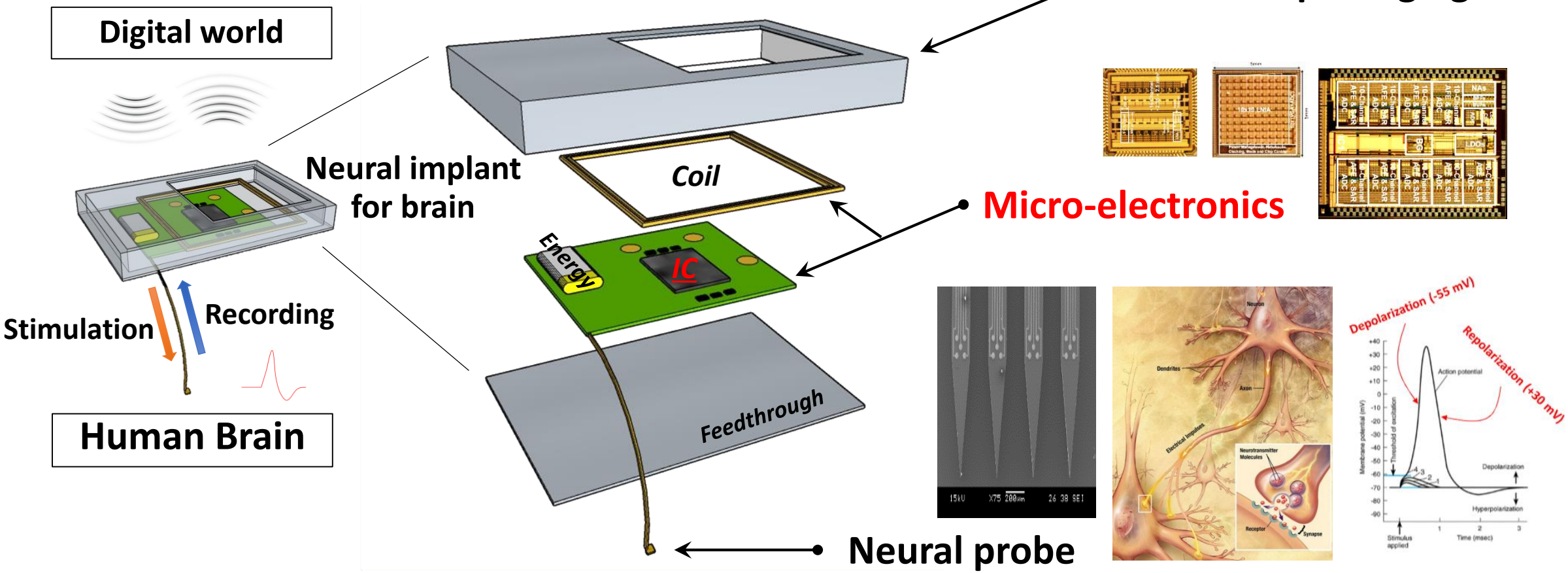
Fig. 1. *A wide variety of devices are in various stages of development, from feasibility studies to clinical trials to marketed products.*

Pacemaker
FDA 1986

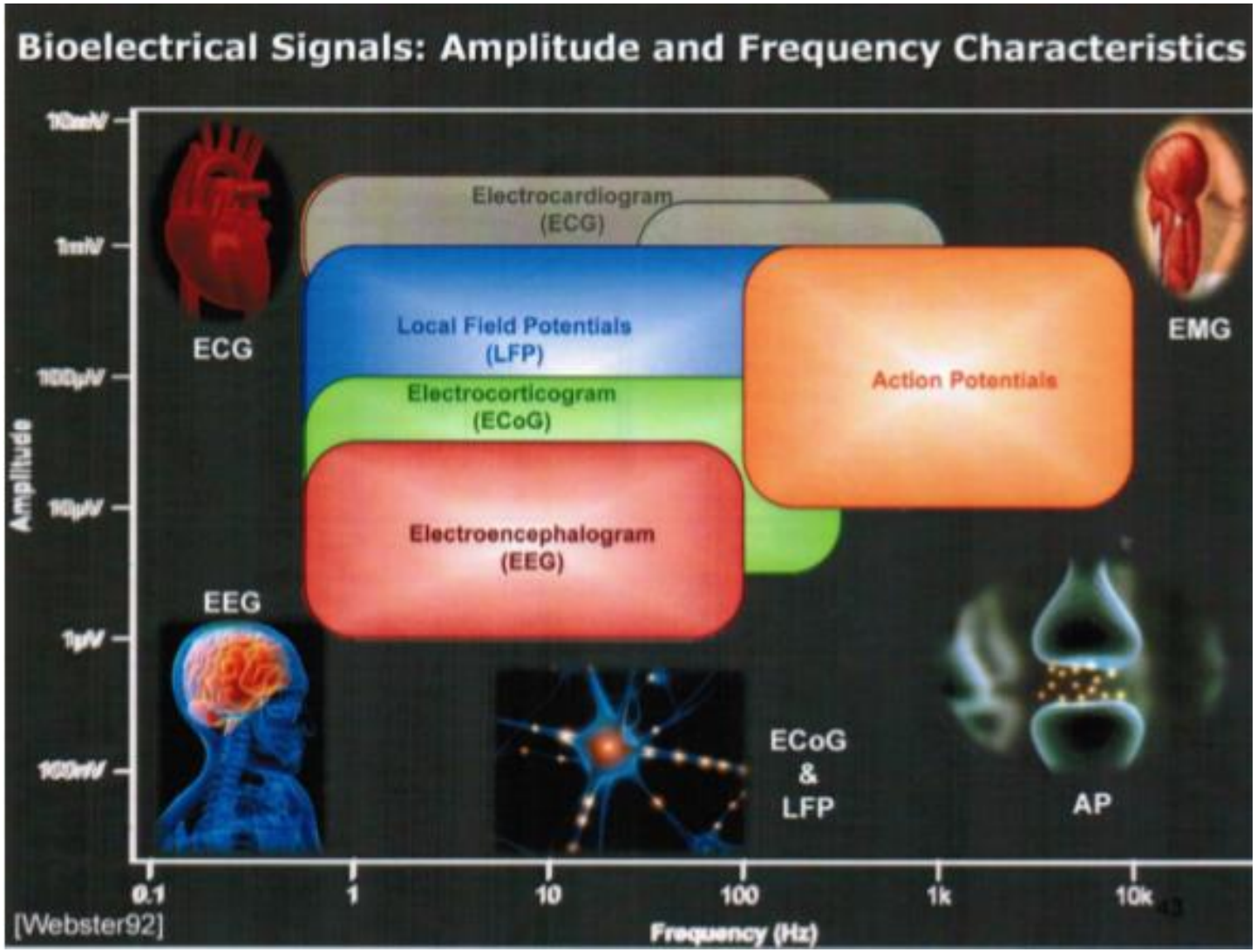
Spinal cord implant
FDA 2005

Brain implant
FDA IDE 2003

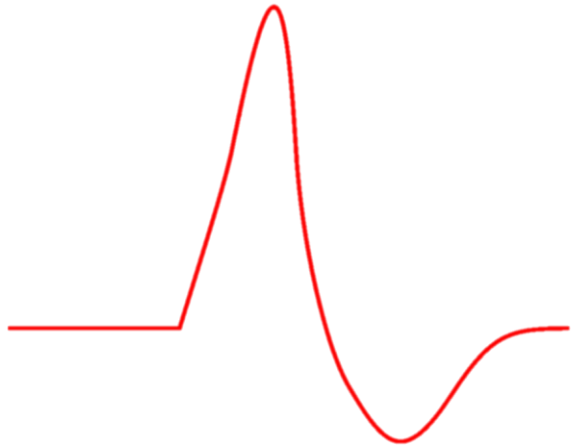
Key Technologies and Components in Neural Implant
植入式神经器件中的关键技术和组件



Recording – Neural Signal Characteristics
神经信号采集 – 信号特征



Typical Action Potential (AP):
10 – 1000 μV Amplitude
300 – 10k Hz Bandwidth
10M Ω probe impedance



Webster, 1992

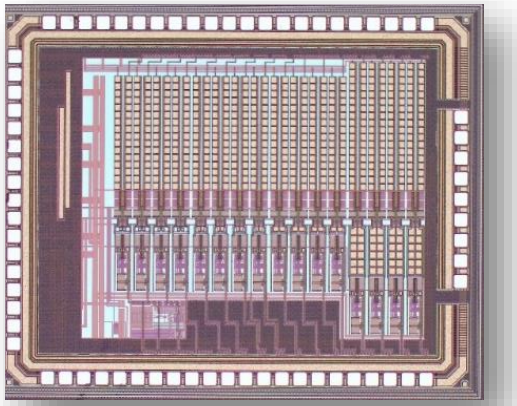
Neural Recording Amplifier – Key Specifications
神经信号放大器 – 关键性能参数

Parameters	Typical value
Input referred noise (IRN)	< 5μ Vrms
Gain	> 60 dB
Bandwidth	1 – 300 Hz (LFP) 100 Hz – 10k Hz (AP)
Input impedance	> 100M Ω (1k Hz), > 10G Ω (DC)
Power consumption	< 10μW per channel
CMRR	> 70 dB

SITRI

SITRI's First Neural Chip NR1
工研院首颗神经芯片NR1

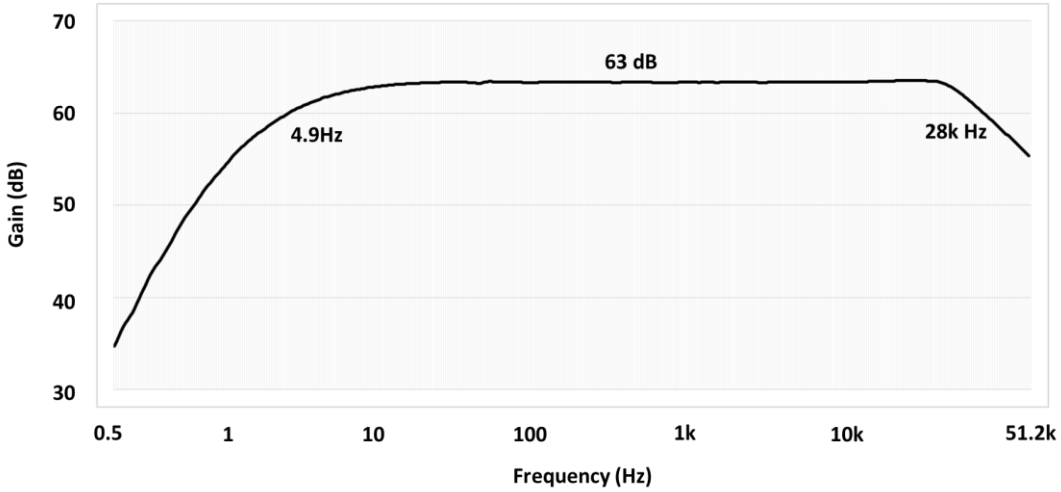
16 channels neural recording IC in SMIC018 GE 1.8/3.3 process (2019Q2)

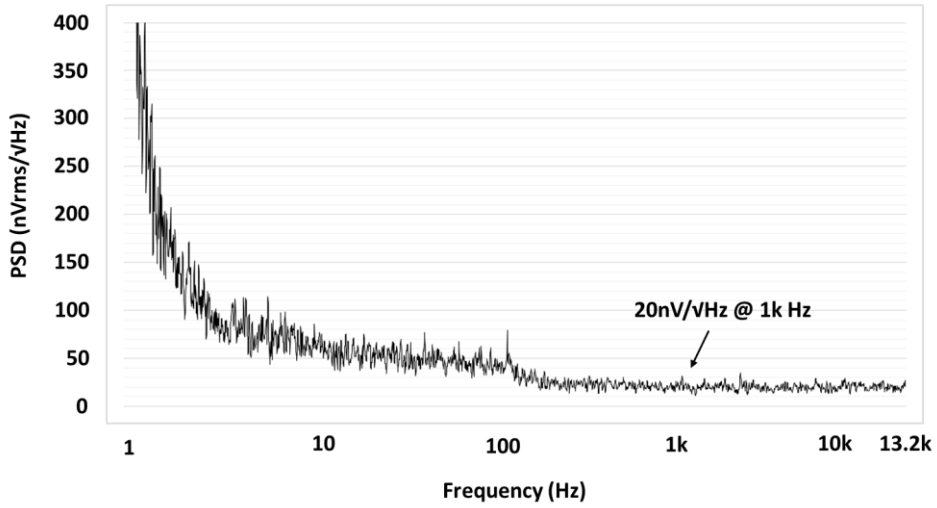


1.7mm x 2.3mm

Key performance:

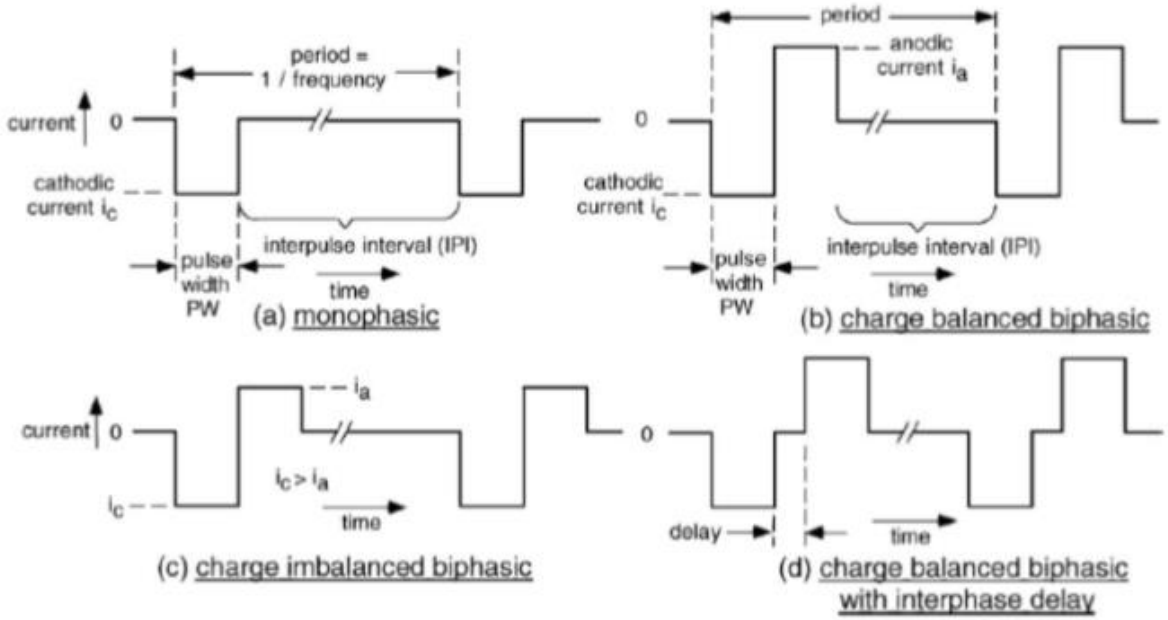
- 16 channels
- 20 µA per channel
- 1.6 µVrms input referred noise (0.3 – 10k Hz)
- 63dB gain
- 5 Hz – 28k Hz Bandwidth
- 200M Ohm impedance @ 1k Hz & 15G @ DC





Stimulation – Requirement
神经刺激 – 功能要求

Typical stimulation waveform:



*D.R. Merrill, Journal of Neuroscience Method, 2005

- **Efficacy**
- **Safety**
- **Low power**

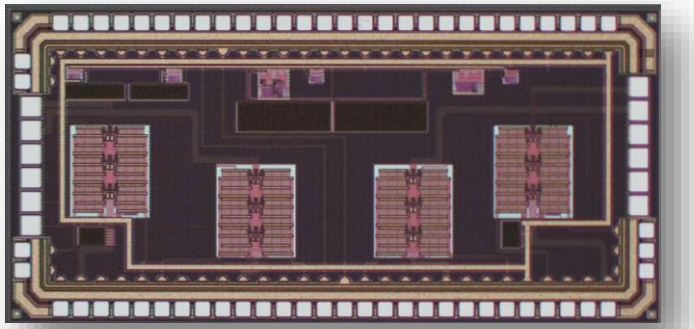
Neural Stimulation AFE – Key Specifications
神经刺激前端电路 - 关键性能参数

Parameters	Value
Voltage rating	> 10V
Current range	10μA – 1mA
Frequency	10 Hz – 1M Hz
Power consumption	< 10μW per channel
Control DAC bits	> 5

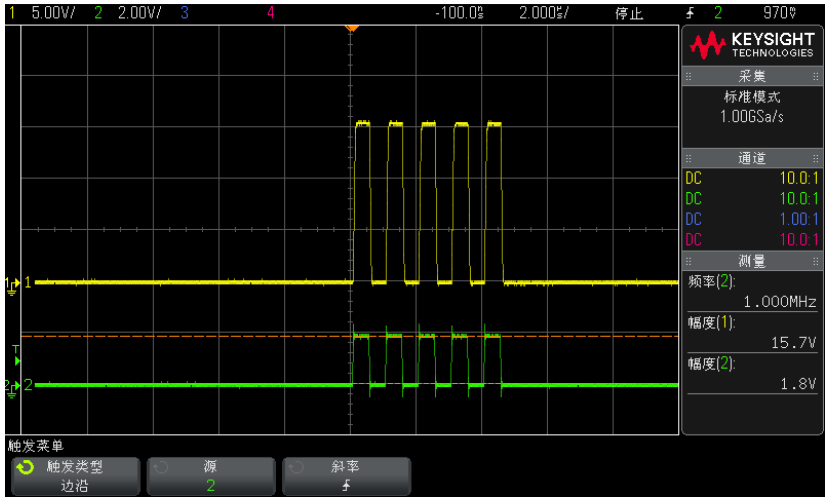
SITRI

SITRI's Stimulation Chip NS1
工研院神经刺激芯片NS1

16V Neural Stimulation IC SMIC018 GE 1.8/3.3 process (2019Q2)



1.2mm x 2.4mm



Key performance:

- 4 channels
- 16V compliance voltage in standard CMOS
- 5 µA Iq per channel @ 100k Hz pulsing
- 10 bits current steering DAC
- 5 µA – 10 mA current output
- Maximum 2M Hz pulsing frequency

SITRI

Available Blocks and Roadmap of AMIC Department
AMIC部门提供的IC模块和技术路线图

		2019	2020	Future
Signal Chain	Low noise amplifier	15nV/√Hz charge amp. 10nV/√Hz voltage amp.	4nV/√Hz charge amp. 2nV/√Hz voltage amp.	< 1nV/√Hz amp.
	ADC	1M 12bits SAR ADC 10k 18 bits ∑-Δ ADC	1M 16 bits SAR ADC 22 bits ∑-Δ ADC 200M pipeline ADC	50M 14 bits SAR ADC 24 bits ∑-Δ ADC
HV Driving Front-End	Voltage pulser	1M 16V pulser 10M 40V pulser	20M 200V pulser	50M 20-200V tunable pulser
	HV DC Gen.	10mA 16V charge pump 10mA 40V Charge pump	1mA 200V charge pump 400mA 5V/12V DCDC	1A/600V DCDC
LV Power Management	LDO	10μW 10mA 1.8V LDO 10μW 10mA 3.3V LDO	10μW 1A 1.8V-4.5V tunable LDO	10μW 1A 1.8V-4.5V tunable LDO
Clock & Reference	Oscillator & PLL	2M-32M CMOS OSC 10ps 1.5G PLL	10M-100M Ring OSC 10k-2M RC OSC 2ps 1.5G PLL	Sub-ps 1.5G PLL

Silicon proven In development (Schematic/GDS) On paper Differentiator

SITRI

Technical Trends in IC Design for Neural Implant
植入式神经器件中的IC设计技术趋势

- **Higher channel counts**
- **Ultrasonic data and power link**
- **Multi-modality recording/stimulation e.g. optical**

Summary
总结

- Neural implant background
- Key technologies and components for neural implant
- SITRI's neural chips
- Technical trends in IC design for neural implants

SITRI

THANK YOU

More than Moore · More than Innovation

SITRI

lei.yao@sitrigroup.com